AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY
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Faculty of Computer Science, Electronics and Telecommunications
DEPARTMENT OF ELECTRONICS

ELECTRONIC DEVICES

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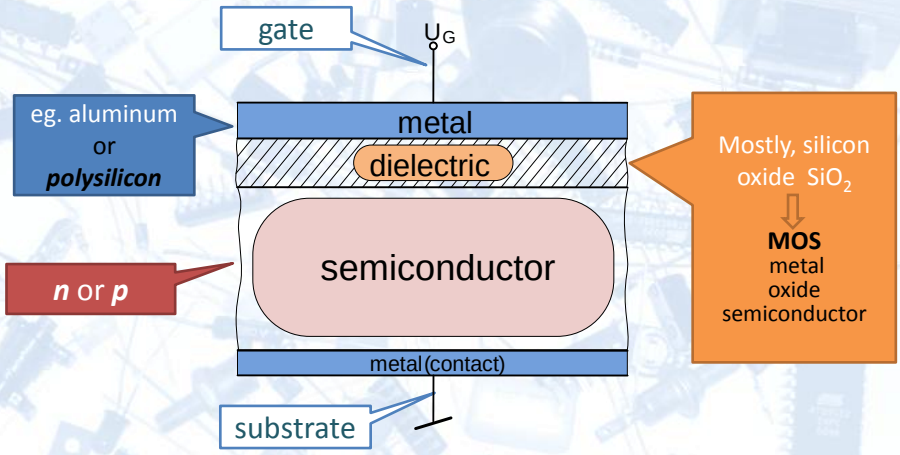
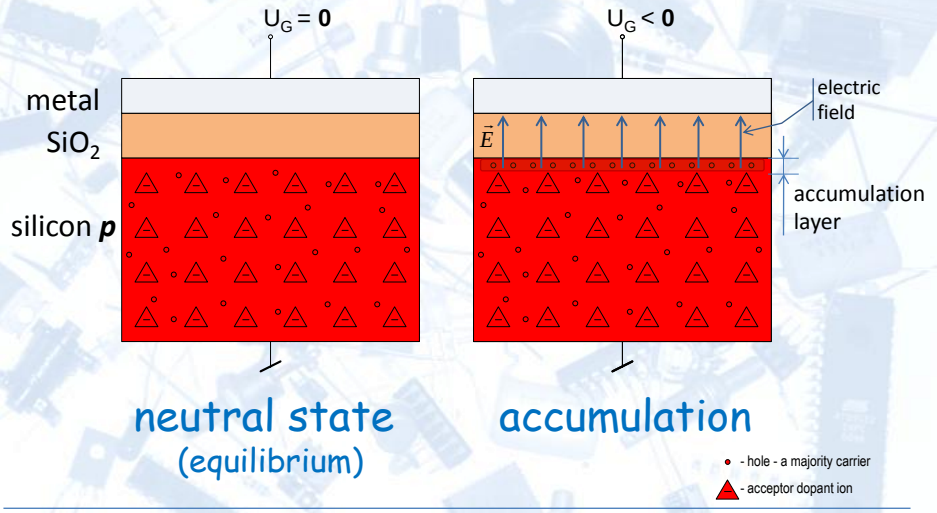
METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR

MOSFET

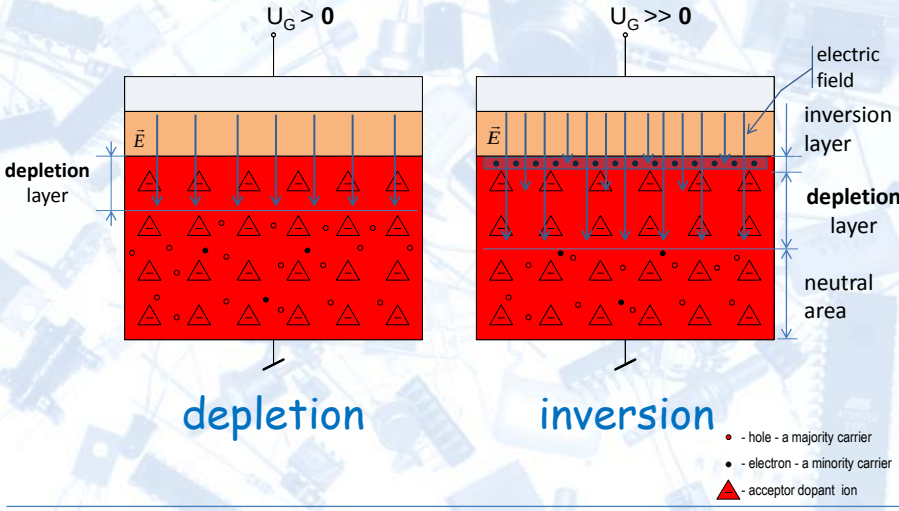
structure
METAL-INSULATOR-SEMOCONDUCTOR (MIS)



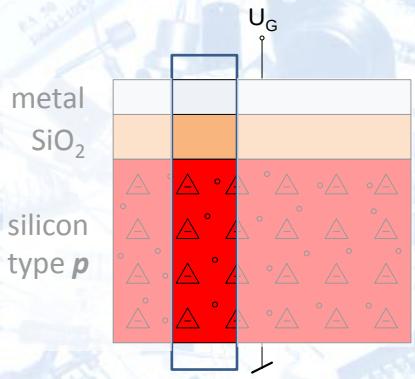
MOS structure
POLARIZATION



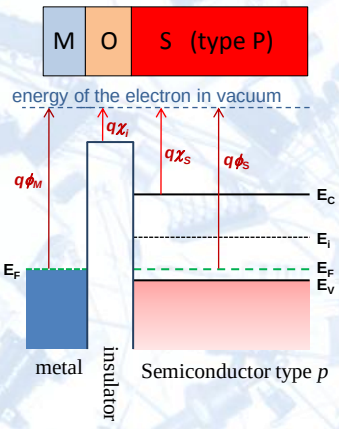
MOS structure
POLARIZATION



MOS structure
ENERGY MODEL



MOS structure
ENERGY MODEL



- Work function W – the energy required to transfer an electron from the Fermi level to infinity (W_∞ - W_F), (free electron in vacuum)

  $q\phi_M$, $q\phi_S$

- Electron affinity χ - determines the work function from the level of the minimum energy in the conduction band E_C

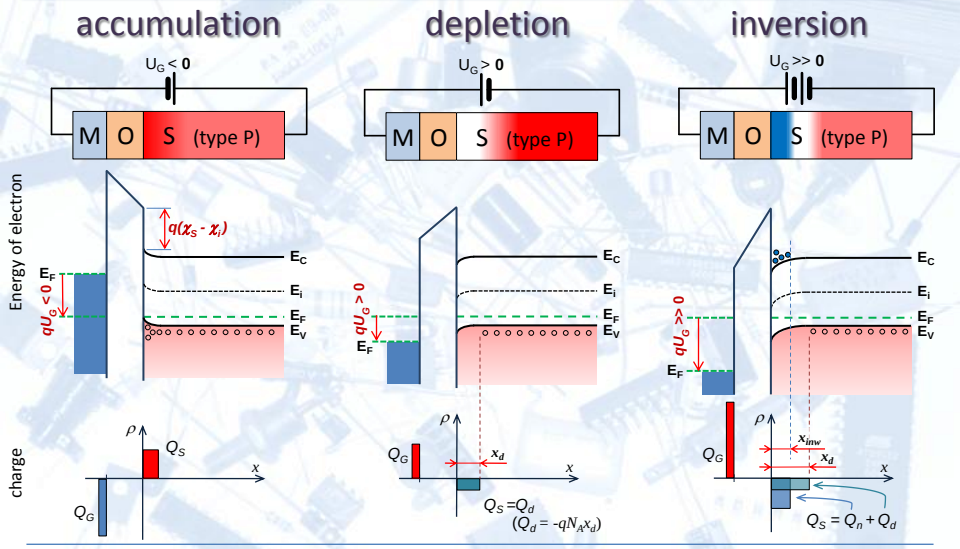
  $q\chi_i$, $q\chi_S$

- ϕ_M – work function potential from metal
- ϕ_S – work function potential from semiconductor
- χ_i – electron affinity of insulator
- χ_S – electron affinity of semiconductor

Ideal structure

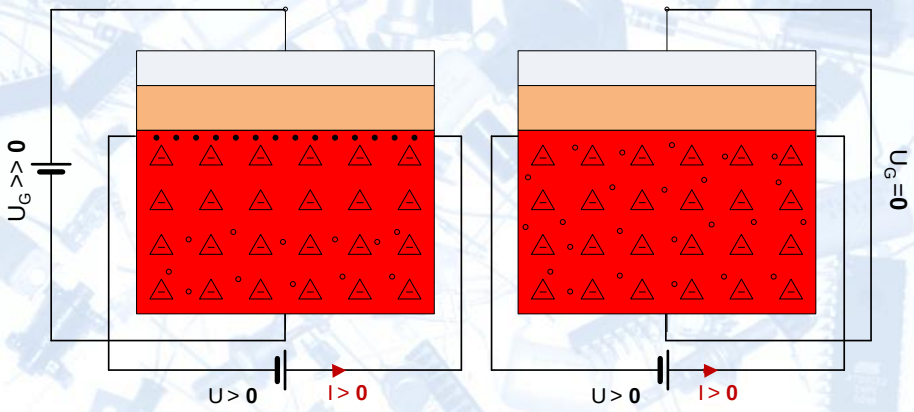
Simplification: - equal work functions of metal and semiconductor (ϕ_M, ϕ_S) – the same Fermi levels
- omitted surface states at the border of the dielectric-semiconductor (surface charge)
- homogeneous insulator - omitted charge in the insulator

MOS structure
ENERGY MODEL - POLARIZATION



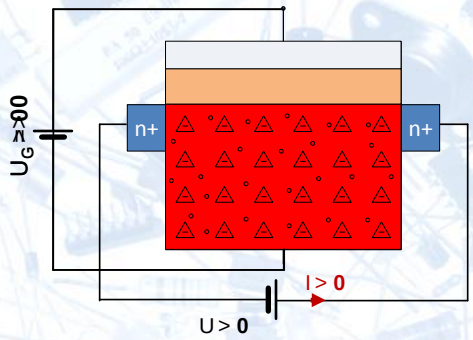
MOS TRANSISTOR

Let's make a transistor



Current flows. But there is no control possibility.

MOS TRANSISTOR



another diode

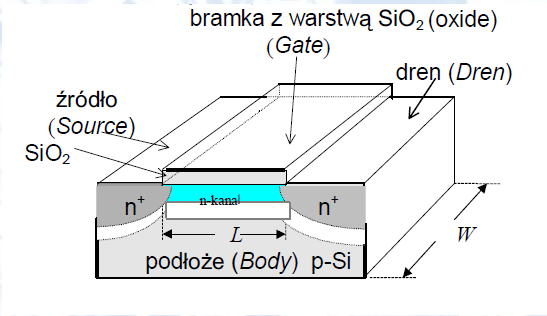
We need a kind of one-directional valve - **diode**

It is OK.

Current flows only when there are electrons under the gate – there is a channel
Gate voltage U_G can control the current by changing the thickness of the channel

MOS TRANSISTOR -structure

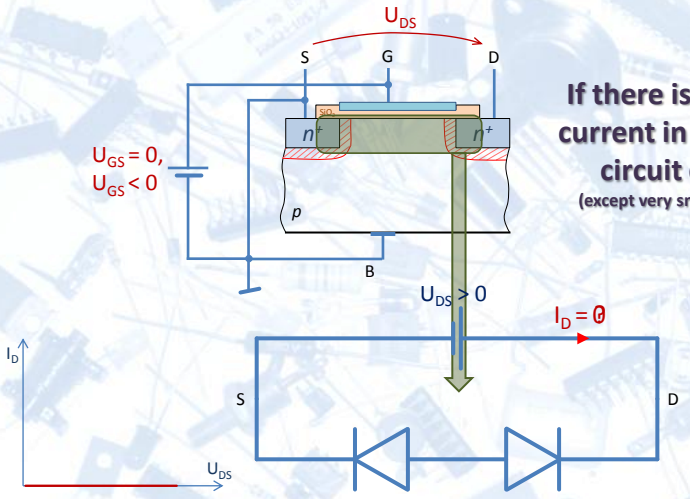
The cross-section of the enhanced MOS transistor, *n* type channel



L – channel length
W – channel width

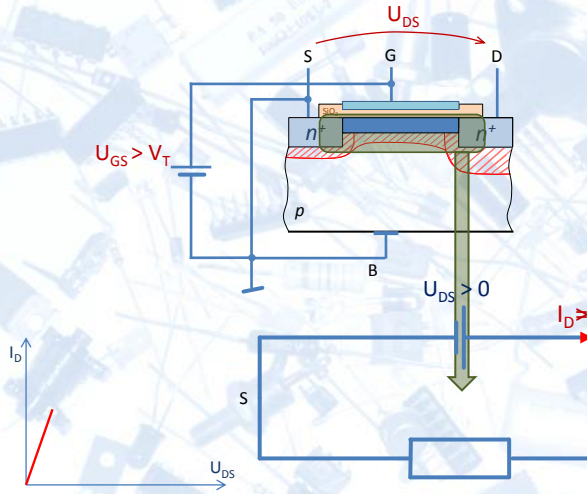
Figure from: S. Kuta „Elementy i układy elektroniczne", AGH 2000

MOS TRANSISTOR
BASICS OF OPERATION



If there is no channel, the current in the drain-source circuit does not flow
(except very small reverse diode current)

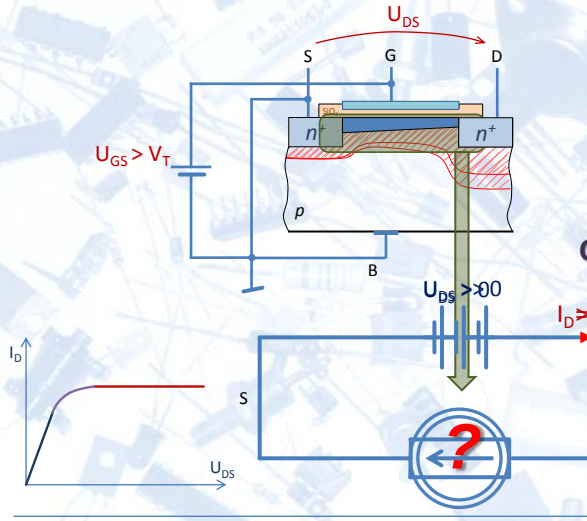
MOS TRANSISTOR
BASICS OF OPERATION



$U_{GS} > V_T$ – inversion:
changes of U_{GS} cause modulation channel conductance thus controlling drain current

LINEAR OPERATION

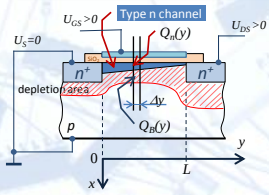
MOS TRANSISTOR
BASICS OF OPERATION



pinch-off
$U_{DS} = U_{GS} - V_T$
increasing of U_{DS}
$U_{DS} > U_{GS} - V_T$

SATURATION:
changes of U_{DS} DO NOT CAUSE increasing of drain current

MOS TRANSISTOR
DRAIN CURRENT



L – channel length
W – channel width

One has to integrate the equation (1) „along the channel length", from 0V to U_{DS}:

$$I_D \int_0^L dy = C_{ox}\mu_e W \int_0^{U_{DS}} [U_G - V_T - U(y)]dU \qquad (1)$$

then we get:

$$I_D L = C_{ox}\mu_e W\left[(U_{GS}-V_T)U_{DS} - \frac{U_{DS}^2}{2}\right]$$

and finally:

Linear area

$$I_D = C_{ox}\mu_e \frac{W}{L}\left[(U_{GS}-V_T)U_{DS} - \frac{U_{DS}^2}{2}\right] \qquad (2)$$

When the U_{DS} reaches the value $U_{DS} = U_{GS} - V_T$, then according to (2) drain current would have to decrease(in linear area I_D is proportional to U^2_{DS}). Then at the drain the channel is pinched-off – saturation of I_D takes place. Therefore, substituting ($U_{DS} = U_{GS} - V_T$) to (2) one obtains formula for I_D current in saturation :

Saturation area

$$I_D = C_{ox}\mu_e \frac{W}{L}\left[\frac{(U_{GS}-V_T)^2}{2}\right]$$

For the P-type transistor, the drain current and voltage are negative

MOS TRANSISTOR
OUTPUT CHARACTERISTICS

LINEAR AREA

$U_{GS} > V_{Tn}$

$0V < U_{DS} < U_{GS} - V_{Tn}$

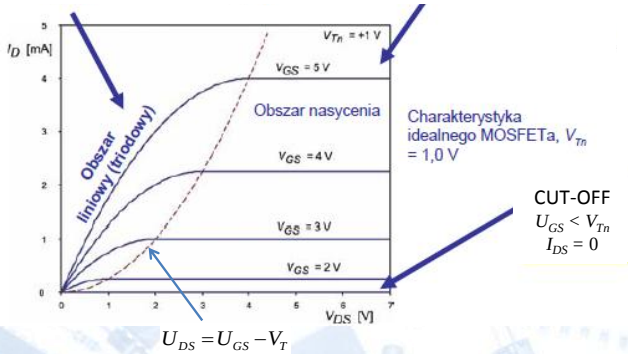
$$I_D = \frac{W}{L}\mu_n C_{ox}\left[(U_{GS}-V_T)U_{DS} - \frac{U_{DS}^2}{2}\right]$$

SATURATION AREA

$U_{GS} > V_{Tn}$

$U_{DS} > U_{GS} - V_{Tn} > 0V$

$$I_D = \frac{W}{2L}\mu_n C_{ox}(U_{GS}-V_T)^2$$

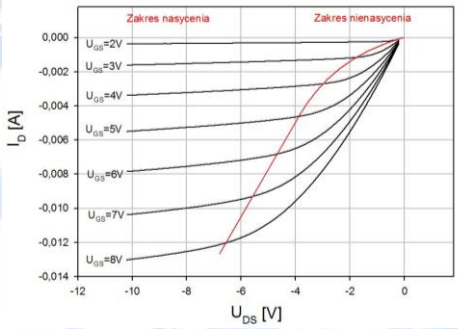


CUT-OFF
$U_{GS} < V_{Tn}$
$I_{DS} = 0$

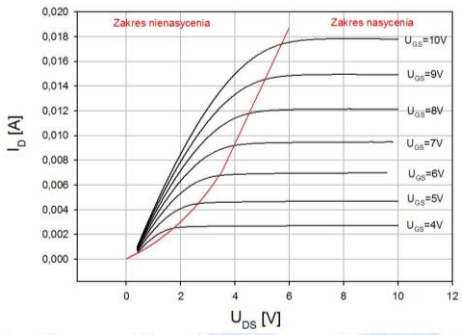
$U_{DS} = U_{GS} - V_T$

MOS TRANSISTOR
OUTPUT CHARACTERISTICS

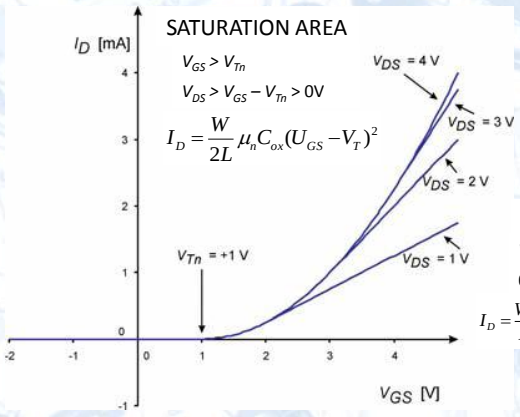
PMOS



NMOS



MOS TRANSISTOR
TRANSFER CHARACTERISTICS



SATURATION AREA

$V_{GS} > V_{Tn}$

$V_{DS} > V_{GS} - V_{Tn} > 0V$

$$I_D = \frac{W}{2L}\mu_n C_{ox}(U_{GS} - V_T)^2$$

LINEAR AREA

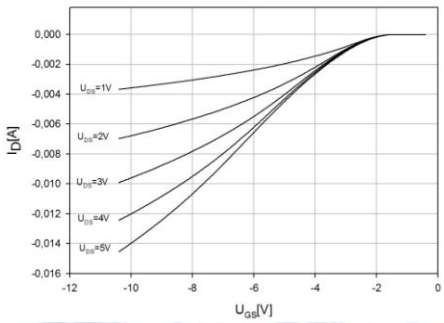
$V_{GS} > V_{Tn}$

$0V < V_{DS} < V_{GS} - V_{Tn}$

$$I_D = \frac{W}{L}\mu_n C_{ox}\left[(U_{GS} - V_T)U_{DS} - \frac{U_{DS}^2}{2}\right]$$

MOS TRANSISTOR
TRANSFER CHARACTERISTICS

PMOS



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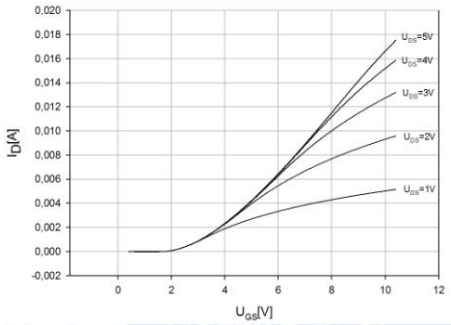
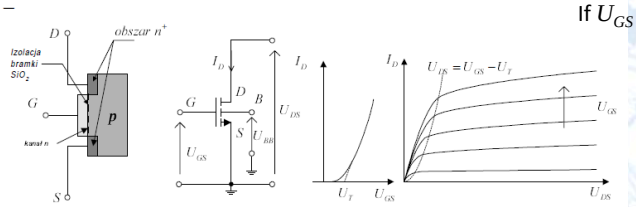


Is it possible for these characteristics to indicate the linear area and saturation?

TYPES OF MOS TRANSITORS

– **enhanced N-channel:** $U_{DS}>0$, $I_D>0$, $U_{GS}>0$ i $U_T>0$

If $U_{GS} = 0$ => no channel



– **enhanced P-channel:** $U_{DS}<0$, $I_D<0$, $U_{GS}<0$ i $U_T<0$

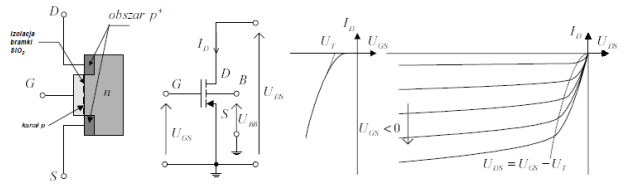
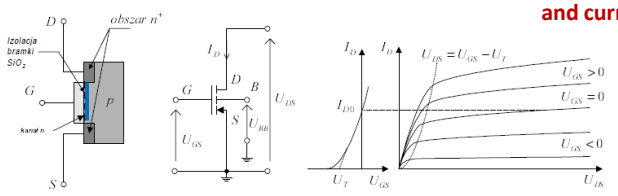


Figure from: S. Kuta „Elementy i układy elektroniczne", AGH 2000

TYPES OF MOS TRANSITORS

depletion N-channel: $U_{DS}>0$, $I_D>0$, $U_{GS}<0$ i $U_P<0$

At $U_{GS}=0$ channel exists and current I_D can flow



depletion P-channel: $U_{DS}<0$, $I_D<0$, $U_{GS}>0$ i $U_P>0$

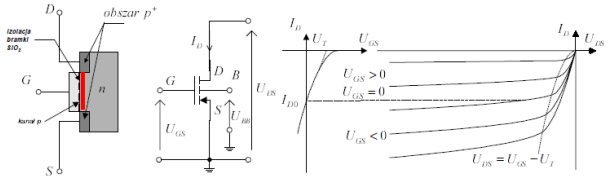


Figure from: S. Kuta „Elementy i układy elektroniczne", AGH 2000

Example

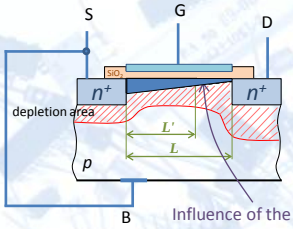
A MOS n-channel transistor has a threshold voltage V_{TN}=1V.

At: V_{DS}=4V and V_{GS}=2V, the I_D=5mA.

What would be the value of I_D,

if U_{GS} increases two times?

MOS TRANSISTOR
CHANNEL LENGTH MODULATION EFFECT



Influence of the U_{DS} increase, channel is getting shorter

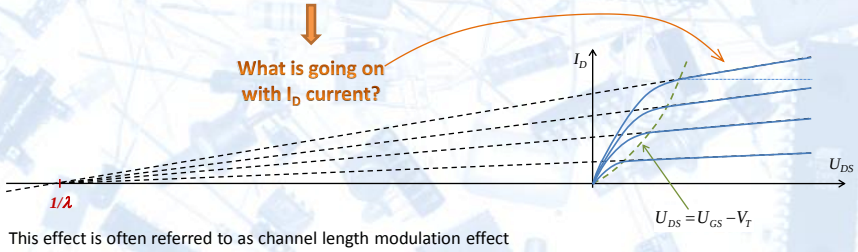
In linear area, it does not appear:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left[U_{GS} - V_T - \frac{U_{DS}}{2}\right]U_{DS}$$

In saturation:

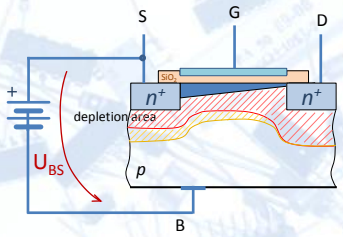
$$I_D = \frac{W}{2L}\mu_n C_{ox}(U_{GS} - V_T)^2(1+\lambda U_{DS})$$

What is going on with I_D current?



This effect is often referred to as channel length modulation effect

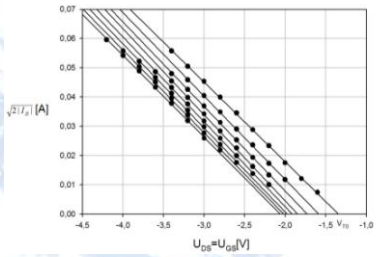
MOS TRANSISTOR
BODY EFFECT



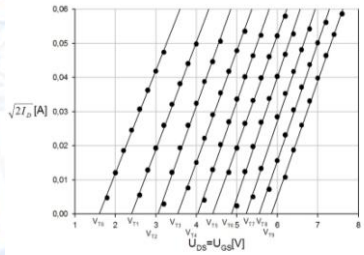
$$V_T = V_{T0} + \gamma(\sqrt{\varphi_s - U_{BS}} - \sqrt{\varphi_s}) \quad \text{for NMOS}$$

γ- bulk coefficient

PMOS

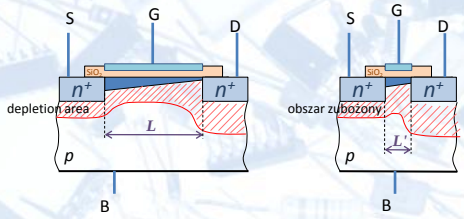


NMOS



MOS TRANSISTOR
other phenomena

- SHORT CHANNEL EFFECT



Shorter channel

↓

depletion areas D-B and S-B are closer to each other, they are „covering" the channel

↓

the share of U_{DS} in creation of channel increases

↓

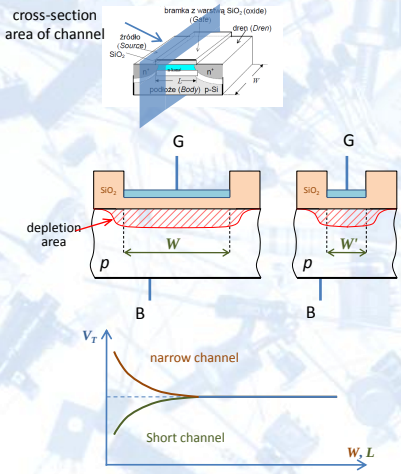
voltage U_{GS} requires less work in order to create the channel

↓

Lower threshold voltage V_T

MOS TRANSISTOR
other phenomena

- NARROW CHANNEL EFFECT



Narrower channel

↓

electric field caused by U_{GS} induce depletion area not only under the gate

↓

channel is getting narrower, thus the share of U_{GS} in inducing depletion area not under the gate increases

↓

voltage U_{GS} requires more work to create channel

↓

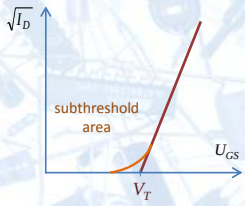
higher threshold V_T

MOS TRANSISTOR
other phenomena

- SUBTHRESHOLD AREA

weak inversion: $\varphi_F \leq \varphi_S < 2\varphi_F$

$$I_D = I_0(U_{GS})\left[1-\exp\left(\frac{-U_{DS}}{\varphi_T}\right)\right]$$



Diffusion mechanism of current flow

MOS TRANSISTOR
EFFECT OF TEMPERATURE

Drain current is affected by temperature dependence:
- mobility of carriers in the channel
- threshold voltage

Temperature coefficient of drain current for saturation range:

$$TWI_D = \frac{1}{I_D}\frac{\partial I_D}{\partial T} = \frac{\partial \mu(T)}{\mu \partial T} - 2\frac{1}{U_{GS}-U_T}\frac{\partial V_T}{\partial T}$$

TWI_D can be positive, negative, or „zero" , depending on the voltage U_{GS}

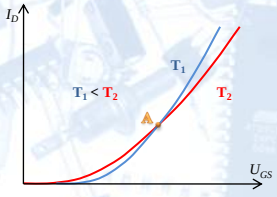
For mobility: $(\mu \sim T^{-a})$:

$$\frac{1}{\mu}\frac{\partial \mu}{\partial T} = -\frac{a}{T}$$

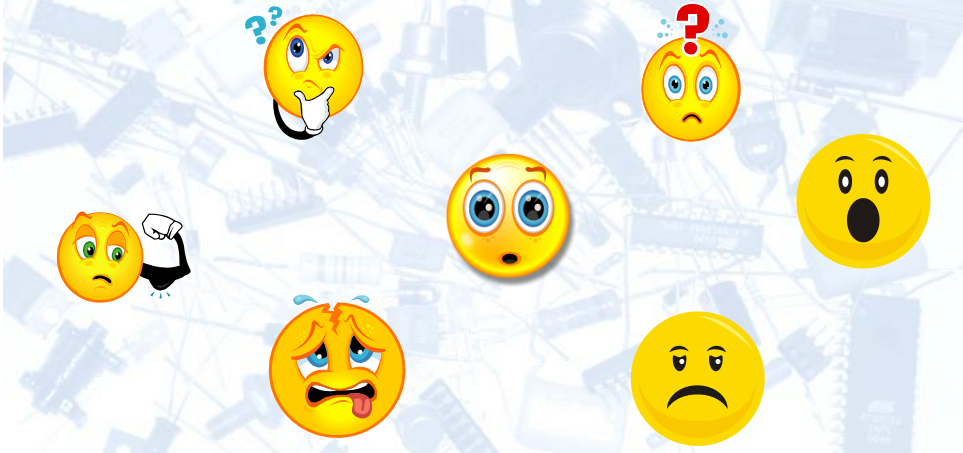
For threshold voltage:

$$V_T = \varphi_m - \chi_S - \frac{E_g}{2q} - \frac{Q_{ef}}{C_{ox}} + \varphi_F + s\gamma\sqrt{|\varphi_F|}$$

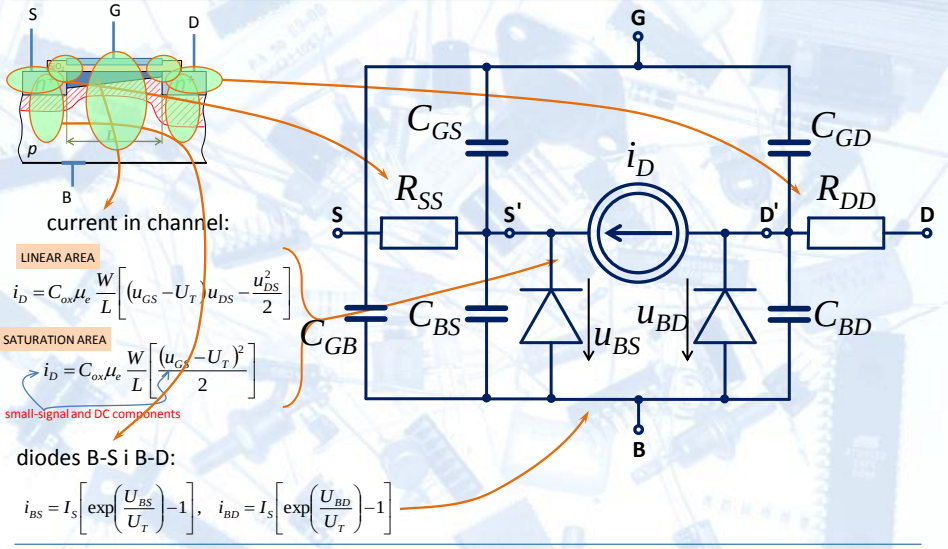
E_g slightly decreases when temperature goes up
φ_F it changes about $-2mV/K$



MOS TRANSISTOR
LARGE-SIGNAL MODEL



MOS TRANSISTOR
LARGE-SIGNAL MODEL



current in channel:

LINEAR AREA

$$i_D = C_{ox}\mu_e \frac{W}{L}\left[(u_{GS}-U_T)u_{DS}-\frac{u_{DS}^2}{2}\right]$$

SATURATION AREA

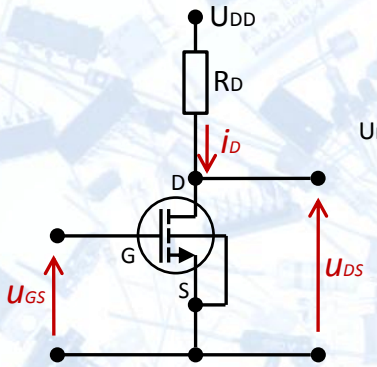
$$i_D = C_{ox}\mu_e \frac{W}{L}\left[\frac{(u_{GS}-U_T)^2}{2}\right]$$

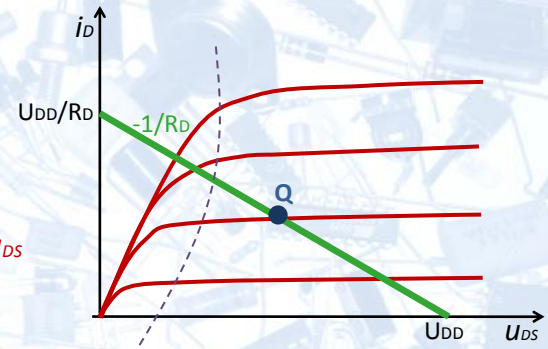
small-signal and DC components

diodes B-S i B-D:

$$i_{BS} = I_S\left[\exp\left(\frac{U_{BS}}{U_T}\right)-1\right], \quad i_{BD} = I_S\left[\exp\left(\frac{U_{BD}}{U_T}\right)-1\right]$$

MOS TRANSISTOR AMPLIFIER

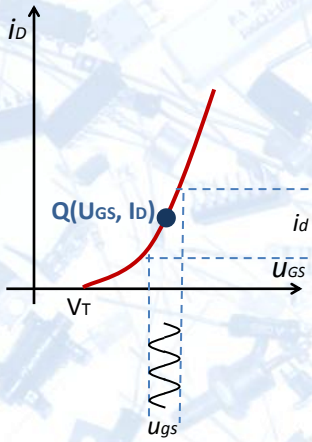


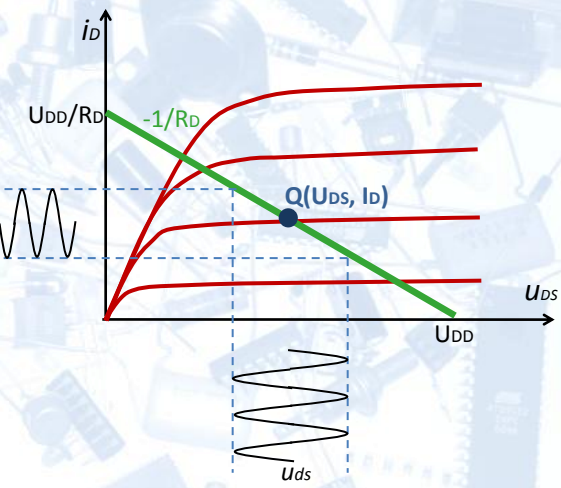


$$i_D = \frac{W}{L}\mu C_{ox}\left(u_{GS} - V_T - \frac{u_{DS}}{2}\right)u_{DS}$$

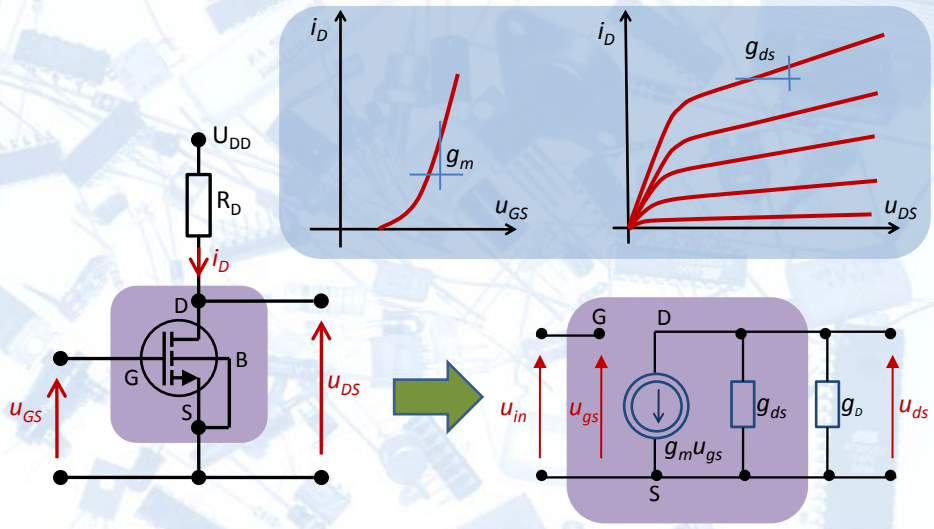
$$i_D = \frac{W}{2L}\mu C_{ox}\left(u_{GS} - V_T\right)^2\left(1 + \lambda u_{DS}\right)$$

MOS TRANSISTOR AMPLIFIER

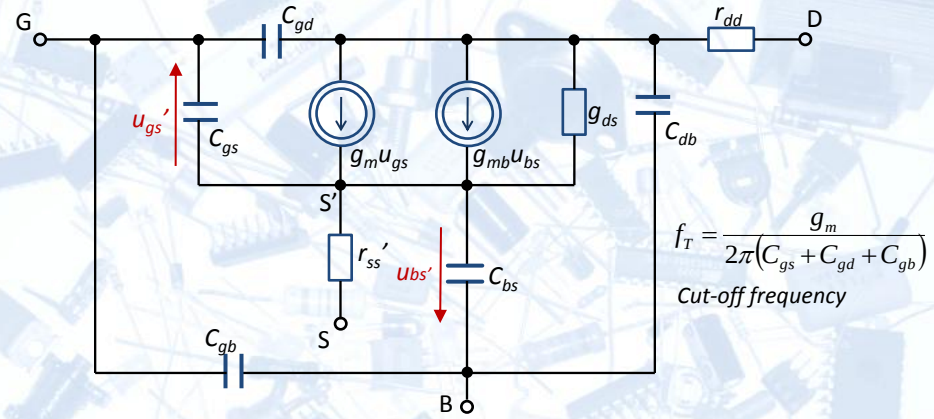




MOS TRANSISTOR
SMALL-SIGNAL MODEL



MOS TRANSISTOR
SMALL-SIGNAL MODEL



$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}+C_{gb}\right)}$$

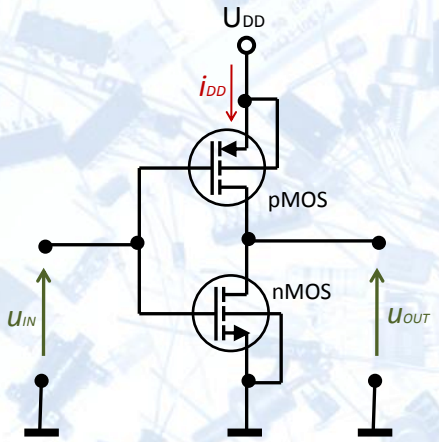
Cut-off frequency

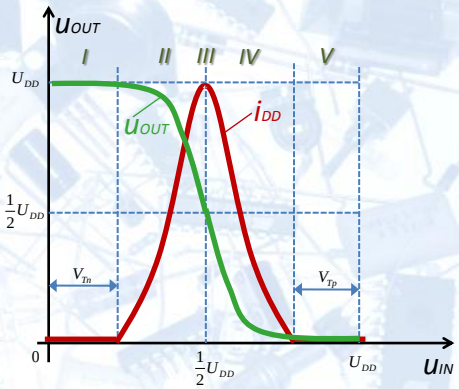
$g_m = \frac{\partial i_D}{\partial u_{GS}} = 2\mu C_{ox}\frac{W}{L}\sqrt{I_D} = \mu C_{ox}\frac{W}{L}\left(U_{GS}-V_T\right)$ - *transconductance* *(for saturation area)*

$g_{ds} = \frac{\partial i_D}{\partial u_{DS}} = \lambda I_D$ - *Output conductance* - *(for saturation area)*

$g_{mb} = \frac{\partial i_D}{\partial u_{BS}} = \frac{\partial i_D}{\partial V_T}\cdot\frac{\partial V_T}{\partial u_{BS}}$ - *transfer body conductance*

CMOS INVERTER





CMOS INVERTER

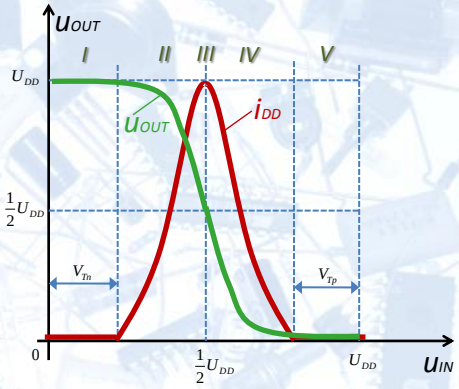
I nMOS – cut-off, pMOS – linear

II nMOS – saturation, pMOS – linear

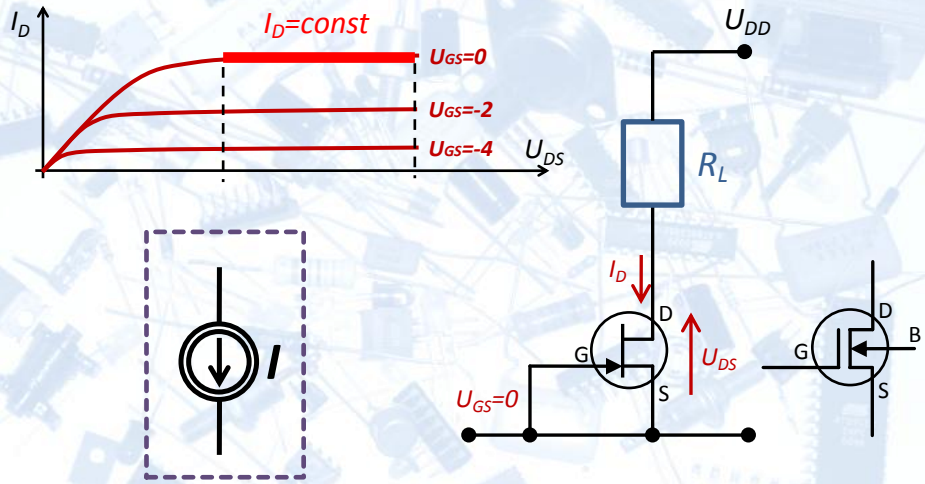
III nMOS – saturation, pMOS – saturation

IV nMOS – linear, pMOS – saturation

V nMOS – linear, pMOS – cut-off

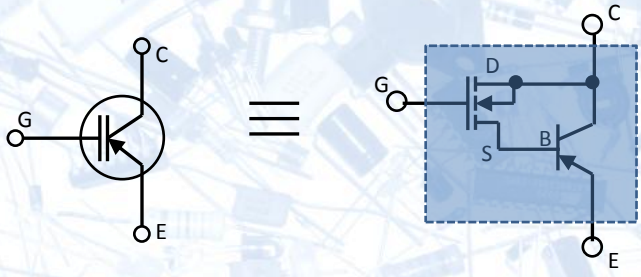


CURRENT STABILIZER



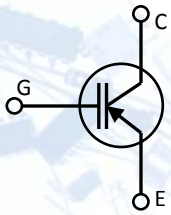
BIPOLAR TRANSISTOR WITH ISOLATED GATE (IGBT)

IGBT – *Insulated Gate Bipolar Transistor*



IGBT transistor combines the positive characteristics of the MOSFETs with the advantages of bipolar transistors

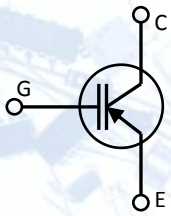
BIPOLAR TRANSISTOR WITH ISOLATED GATE (IGBT)



IGBT

- high input impedance
- ease of control by input voltage
- very small U_{CEsat}
- protected in the event of a short circuit
- low switching losses

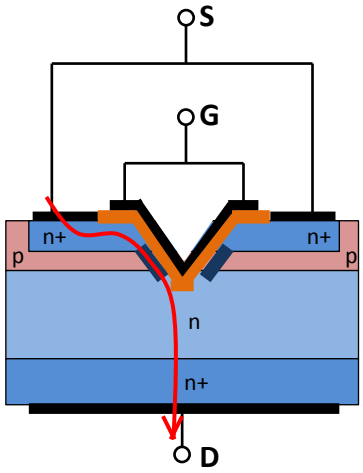
BIPOLAR TRANSISTOR WITH ISOLATED GATE (IGBT)



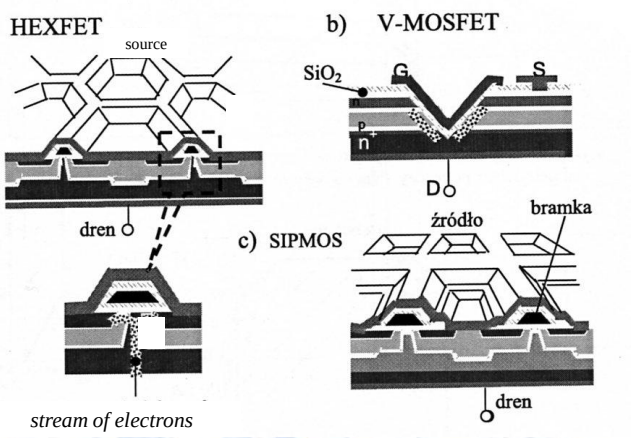
Applications of IGBT

- current sources of high power
- high power converters
- systems with inductive loads
- inverters

VMOS TRANSISTOR



Tranzystory MOS dużej mocy



COMPARISON
BJT VS MOSFET

TRANSCONDUCTANCE

BJT	MOSFET
$g_{m-BJT} = \frac{\partial I_C}{\partial U_{BE}} \cong \frac{I_C}{U_T} \propto I_C$	$g_{m-MOS} = \frac{\partial I_D}{\partial U_{GS}} \cong \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D} \propto \sqrt{I_D}$
- it does not depend on technology	*- It depends on technology*
- it does not depend on dimensions	*- it depends on dimensions*

$$g_{m-BJT} > g_{m-MOS}$$

COMPARISON
BJT VS MOSFET

INPUT IMPEDANCE

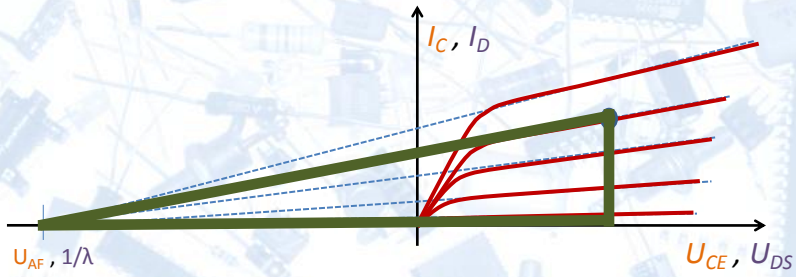
BJT	MOSFET
$r_{be-BJT} = \frac{\beta}{g_m} = \frac{\beta U_T}{I_C}$	$r_{gs-MOS} \Rightarrow \infty$
- very small	

$$r_{be} << r_{gs}$$

COMPARISON
BJT VS MOSFET

OUTPUT IMPEDANCE

BJT	MOSFET
$r_{0-BJT} = \frac{U_{AF} + U_{CE}}{I_C}$	$r_{0-MOS} = \frac{\frac{1}{\lambda} + U_{DS}}{I_D}$



COMPARISON
BJT VS MOSFET

AMPLIFICATION

BJT	MOSFET
$K_{u-BJT} = g_{m-BJT} r_0$	$K_{u-MOS} = g_{m-MOS} r_0$
$K_{u-BJT} = \frac{U_{AF} + U_{CE}}{U_T}$	$K_{u-MOS} = \frac{\frac{1}{\lambda} + U_{DS}}{\frac{U_{GS} - V_{Tn}}{2}} \approx \frac{2}{\lambda (U_{GS} - V_{Tn})}$

if, for example U_{AF}=50V, then K_u=2000

COMPARISON
BJT VS MOSFET

LIMIT FREQUENCY

BJT	MOSFET
$f_{T-BJT} = \frac{g_m}{2\pi(C_\pi + C\mu)} \propto I_C$	$f_{T-MOS} = \frac{g_m}{C_{gs}} \approx \frac{\mu_n}{L^2}(U_{GS} - V_{Tn}) \propto \sqrt{I_D}$

$$f_{T-BJT} > f_{T-MOS}$$