Integrated Circuits and Systems

List of requirements for 2nd test

1. CMOS structure – layout and cross section of whole or part of the gate NOT, NOR or NAND placed on type p or *n substrate*.
2. Layout analysis – schematic extraction from layout, errors and optimalisation.
3. Terms: epitaxy, diffusion, ion implantation, photolithography, metallization.
4. Self-aligned gate in MOS transistor.
5. Technological process: transistor MOS: n-well CMOS, p-well CMOS.
6. Active substrate in CMOS circuits – threats and countermeasures.
7. Simulation of digital CMOS gate work with resistive/capacitance load.
8. Body effect influence on parameters of CMOS gate.
9. Methods of improving time parameters of CMOS gate.
10. Inverter: transfer characteristic, power consumption.
11. Calculation of interconnections' resistance. (resistance per square)
12. Supply lines and interconnections. Rules of designing connections between devices (layers, separation, rules and connections between layers).
13. Design rules (without numerical values).
14. Parasitic capacitances in CMOS circuits.
15. Transmission gate (structure, work, features).
16. Structure of bus buffer.
17. Integrated circuit design flow (with Cadence).
18. Common styles of designing integrated circuits.