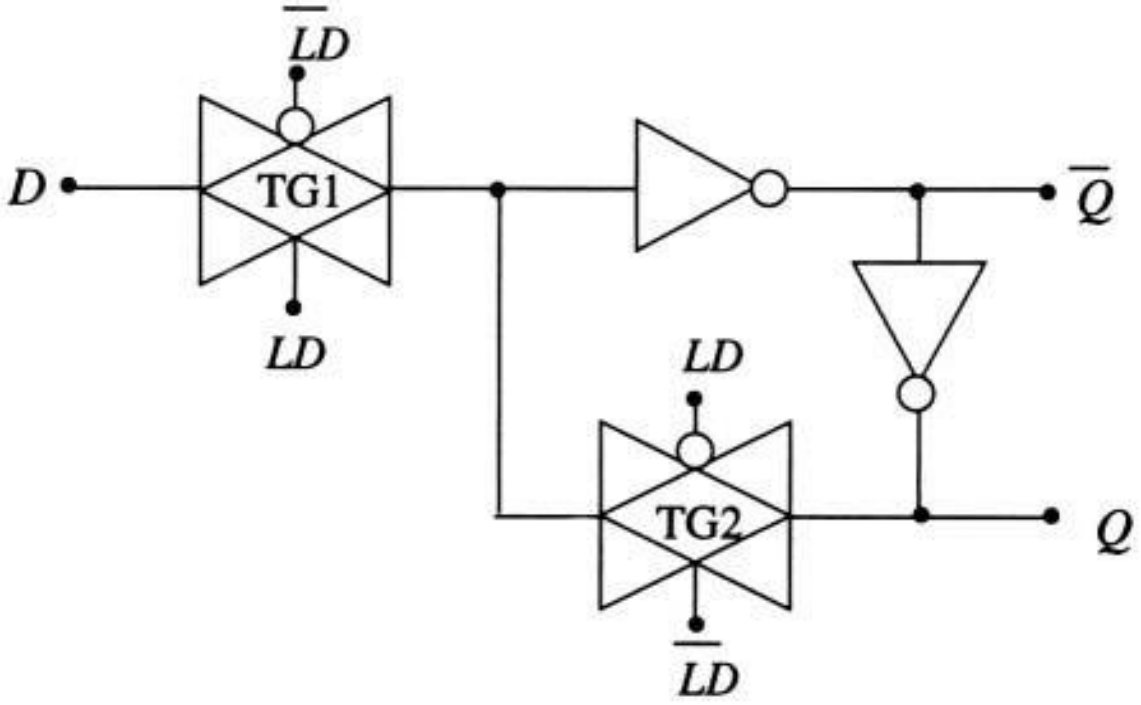
# Digital CMOS circuits

D flip-flop

# D-latch based on transmission gate

D-latch

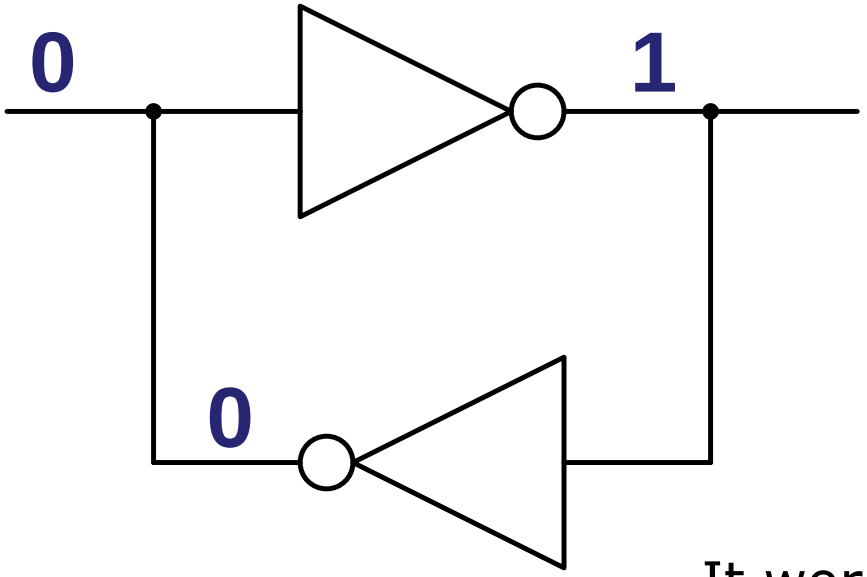



**Why are transmission gates needed in the latch?**

Figures from: John P. Uyemura „CMOS logic circuit design”, Kluwer 2002

# D-latch – work

If there were no transmission gates:



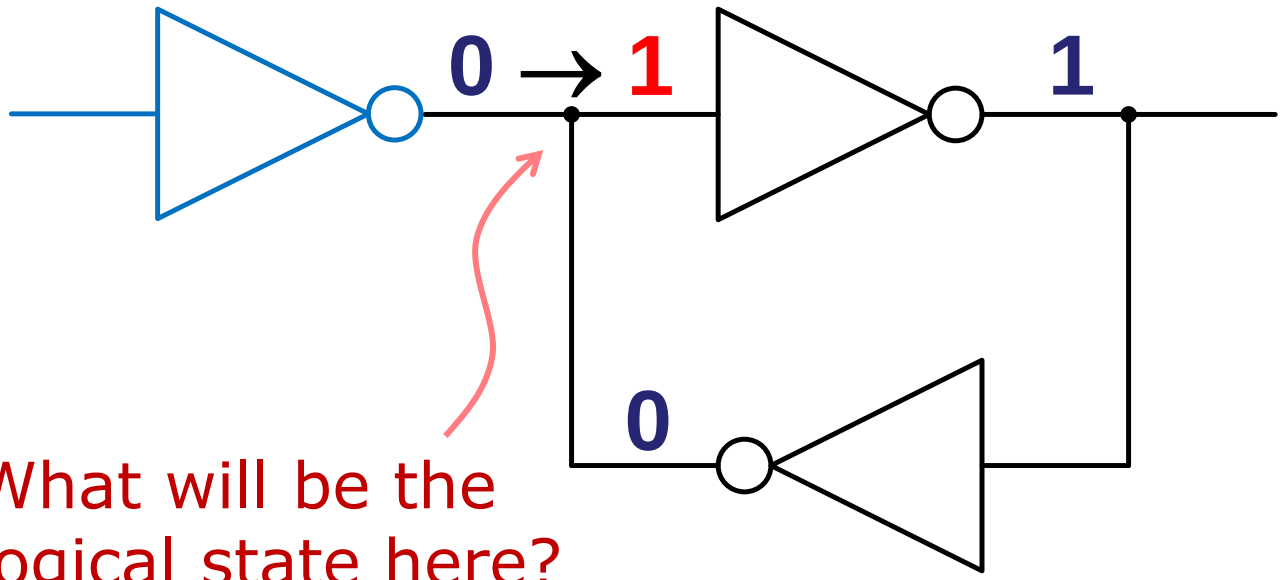

It works as the latch!

**Is there any problem?**

**What about with input?**

# D-latch – work

If there were no transmission gates – driving

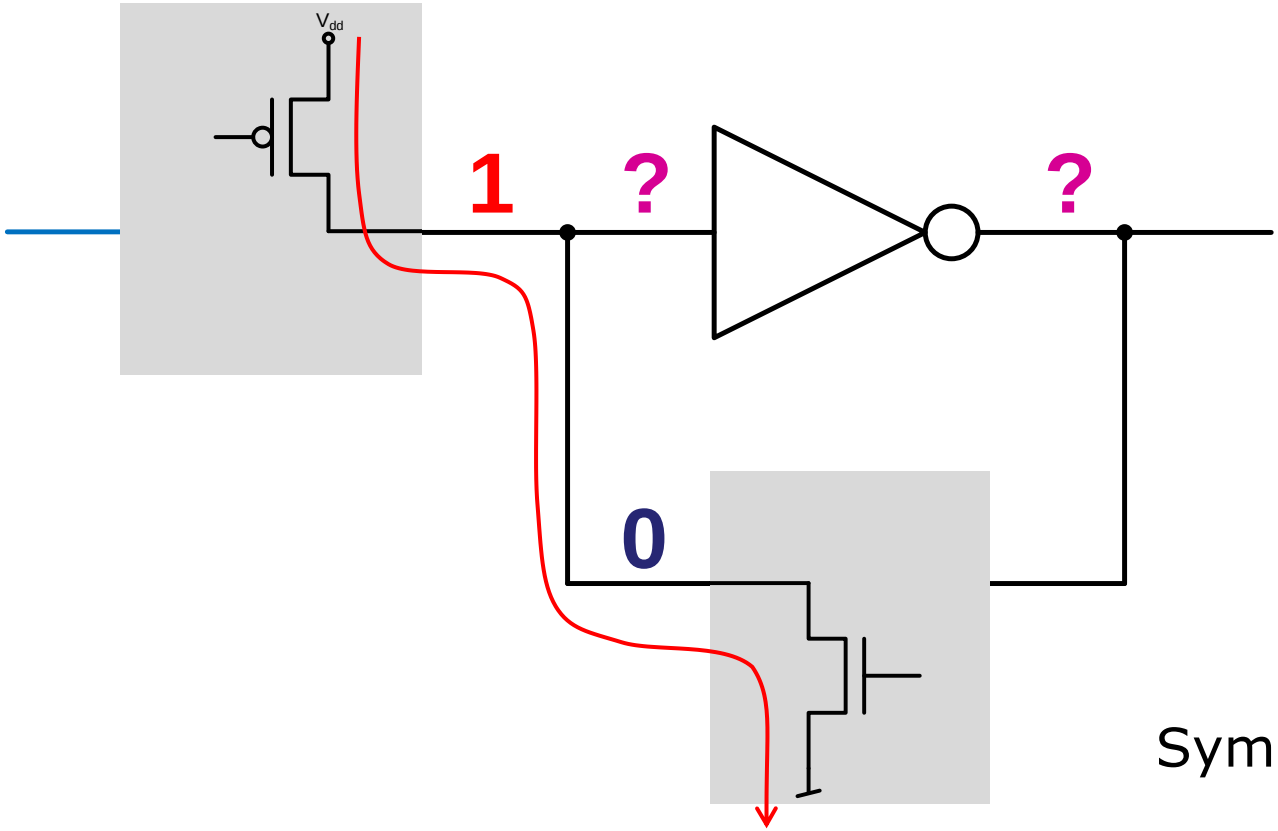



What will be the logical state here?

Symmetrical inverters

# D-latch – work

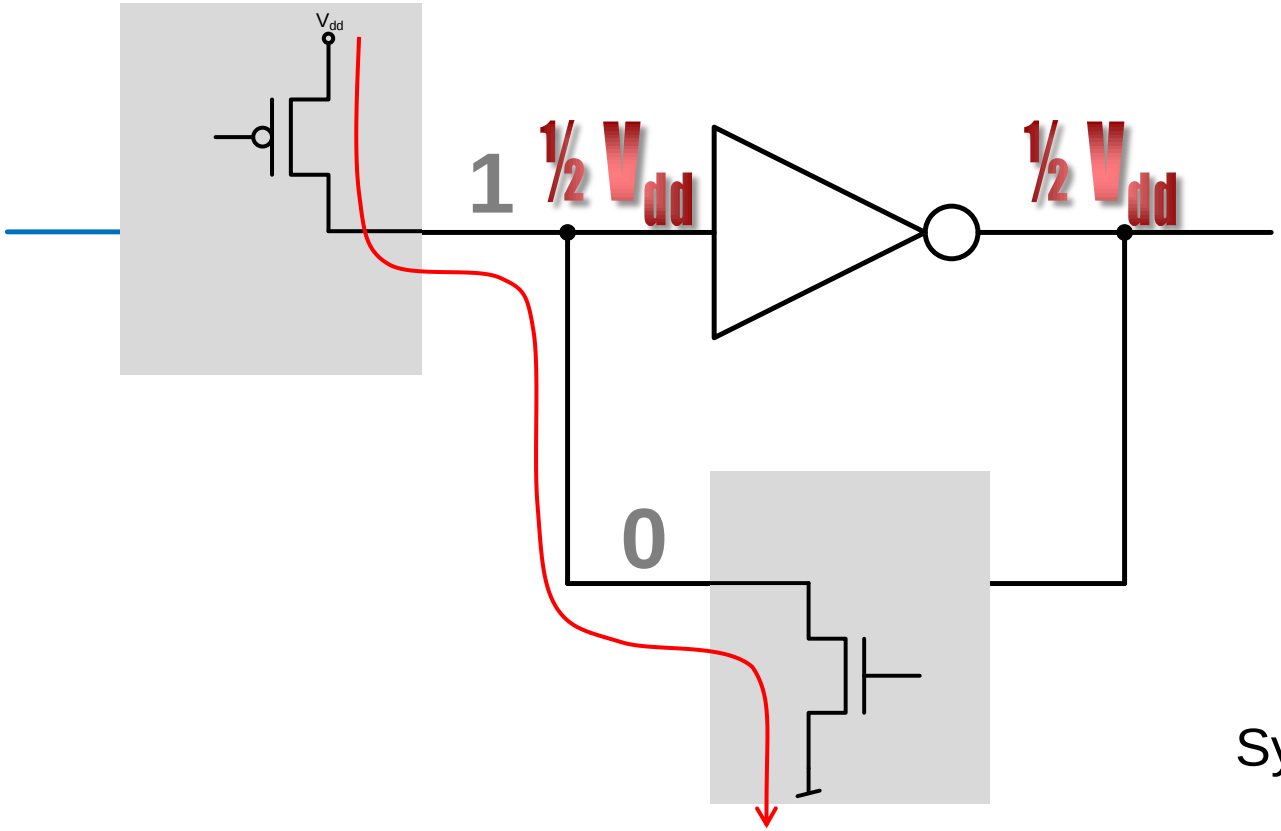
If there were no transmission gates – driving




Symmetrical inverters

# D-latch – work

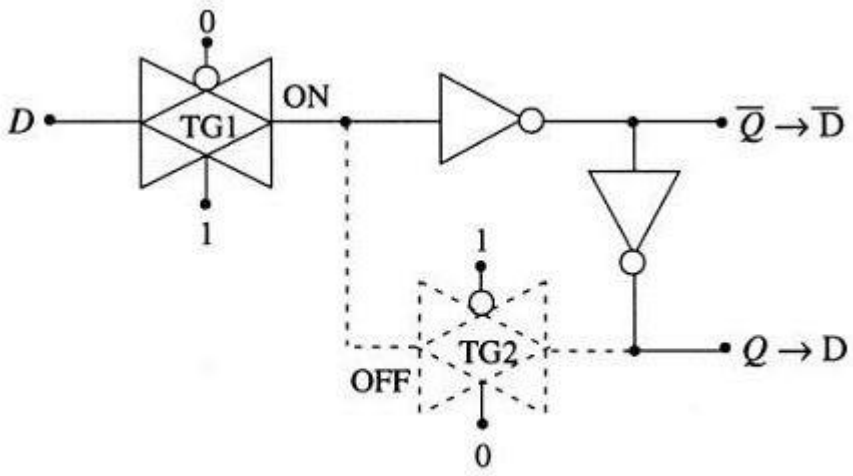
If there were no transmission gates – driving



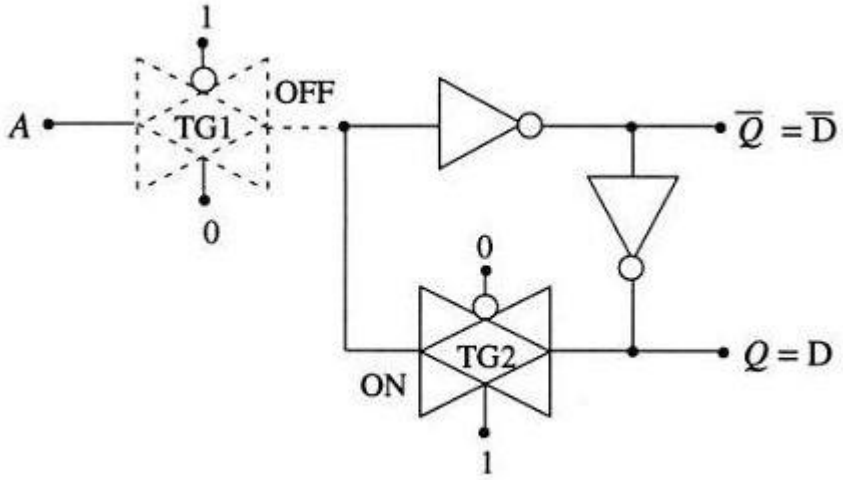

Symmetrical inverters

**Two NOT gates it is not enough, switches are needed –transmission gates.**

# D-latch – work



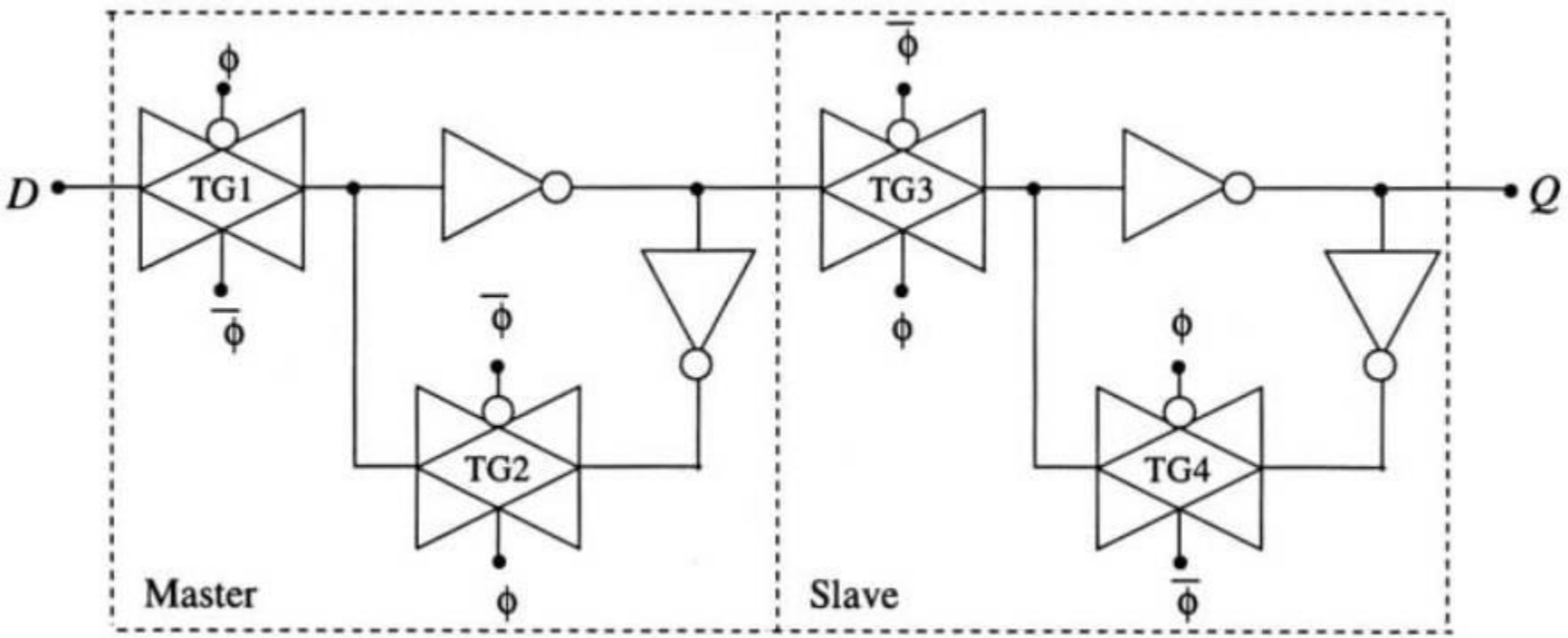

(a) Load operation with *LD*=1




(b) Hold operation with *LD*=0

Figures from: John P. Uyemura „CMOS logic circuit design”, Kluwer 2002

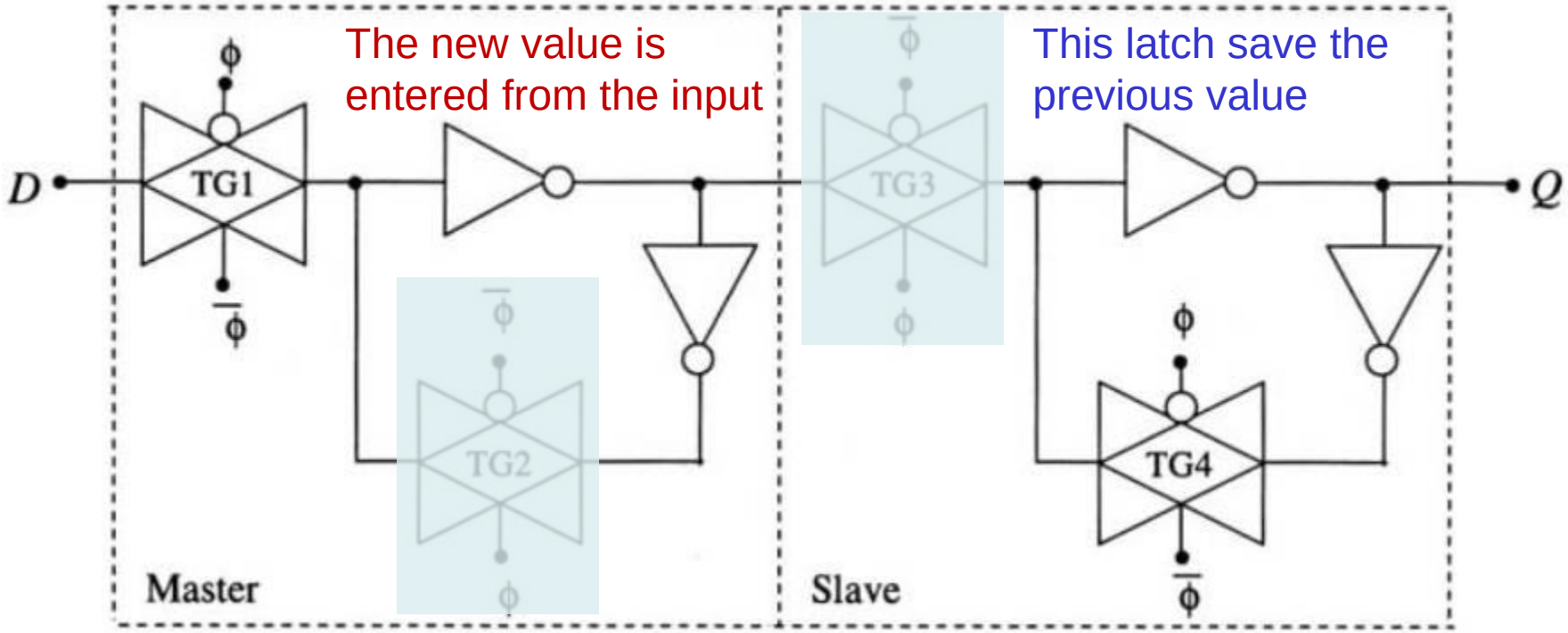
# D flip-flop – schematic




Figures from: John P. Uyemura „CMOS logic circuit design”, Kluwer 2002

# D flip-flop – work

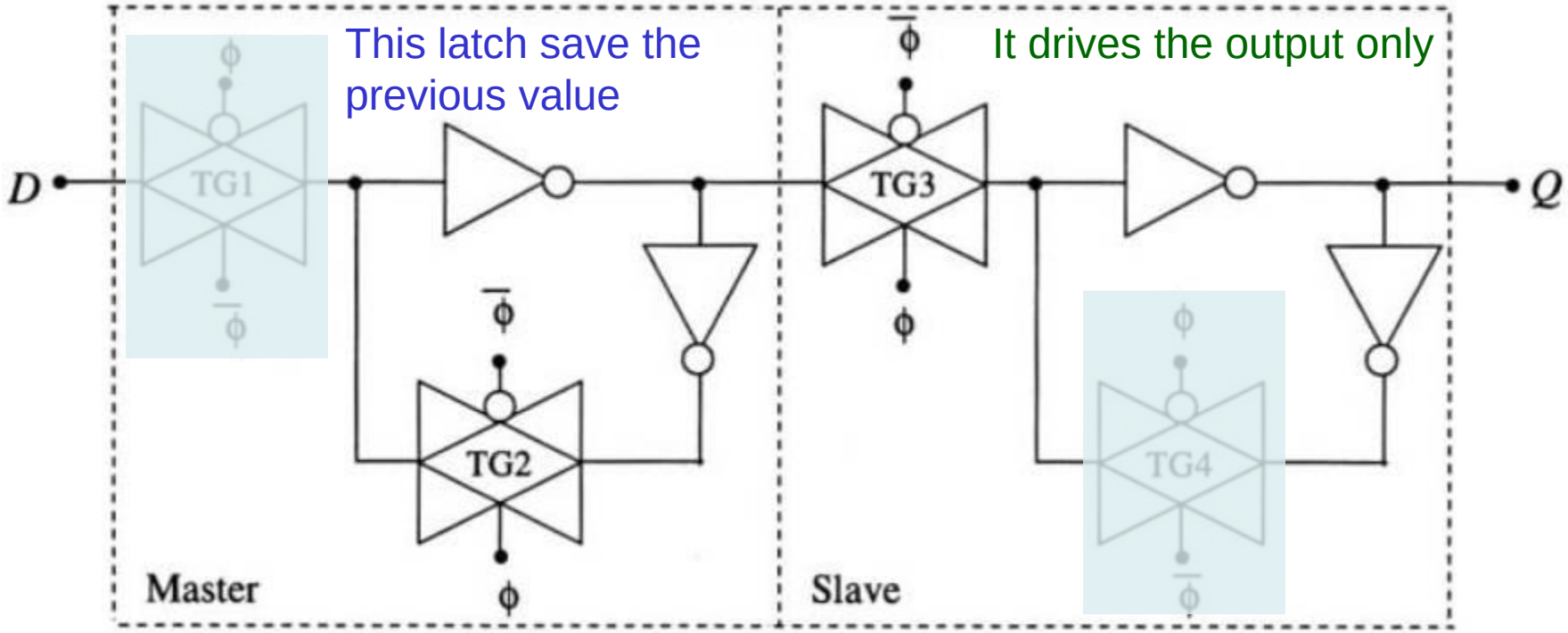
$\phi = 0, \overline{\phi} = 1$ – load




Figures from: John P. Uyemura „CMOS logic circuit design”, Kluwer 2002

# D flip-flop – work

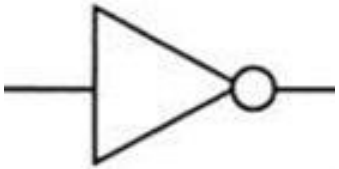
$\phi = 1, \overline{\phi} = 0$ – latching

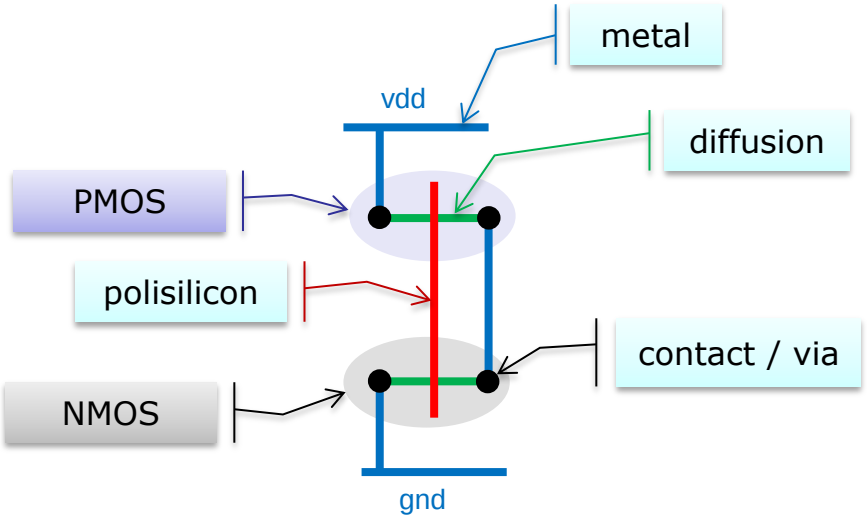


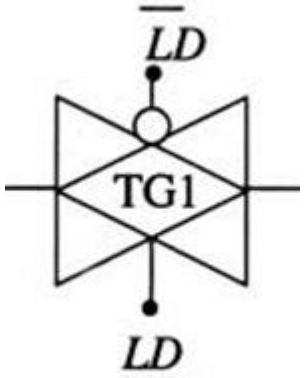

Figures from: John P. Uyemura „CMOS logic circuit design”, Kluwer 2002

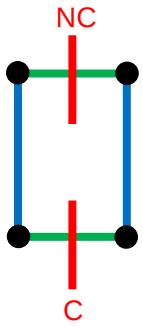
# Layout drawing – the stick diagram

schematic → layout



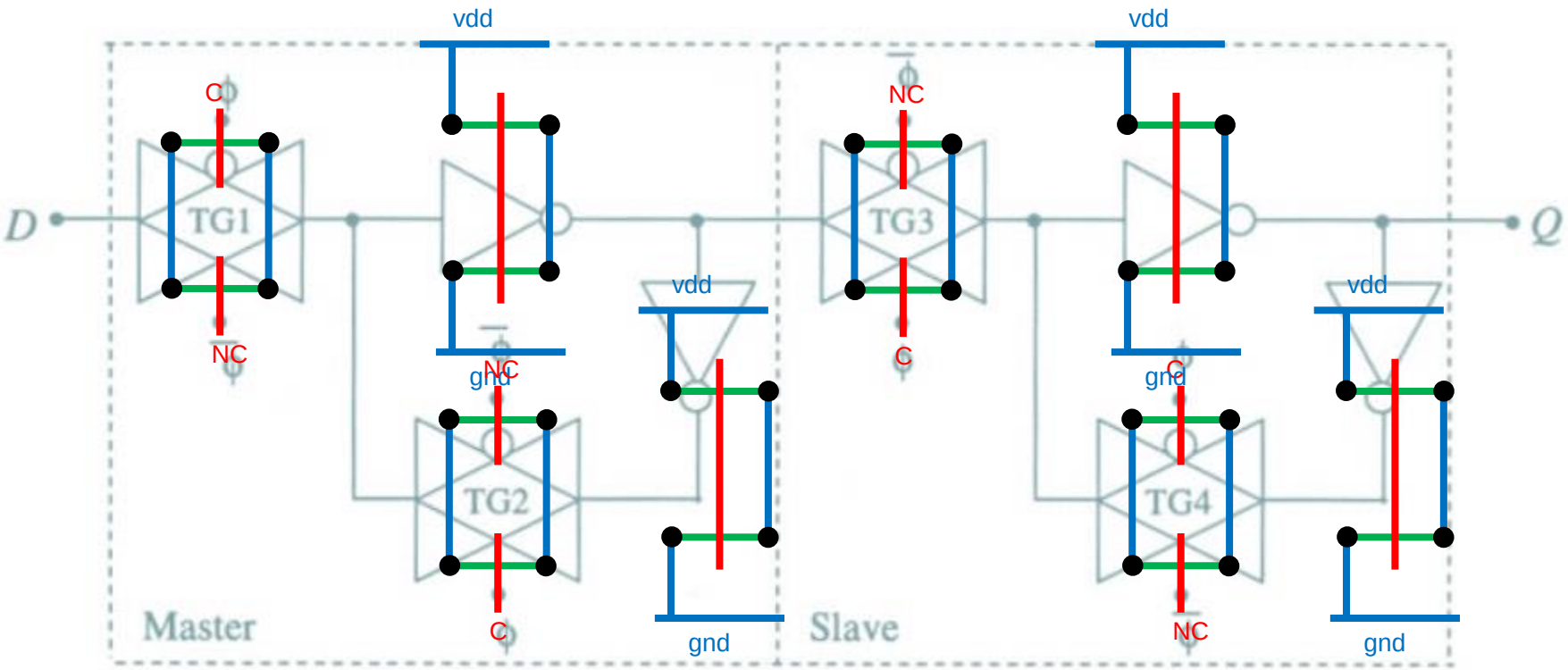


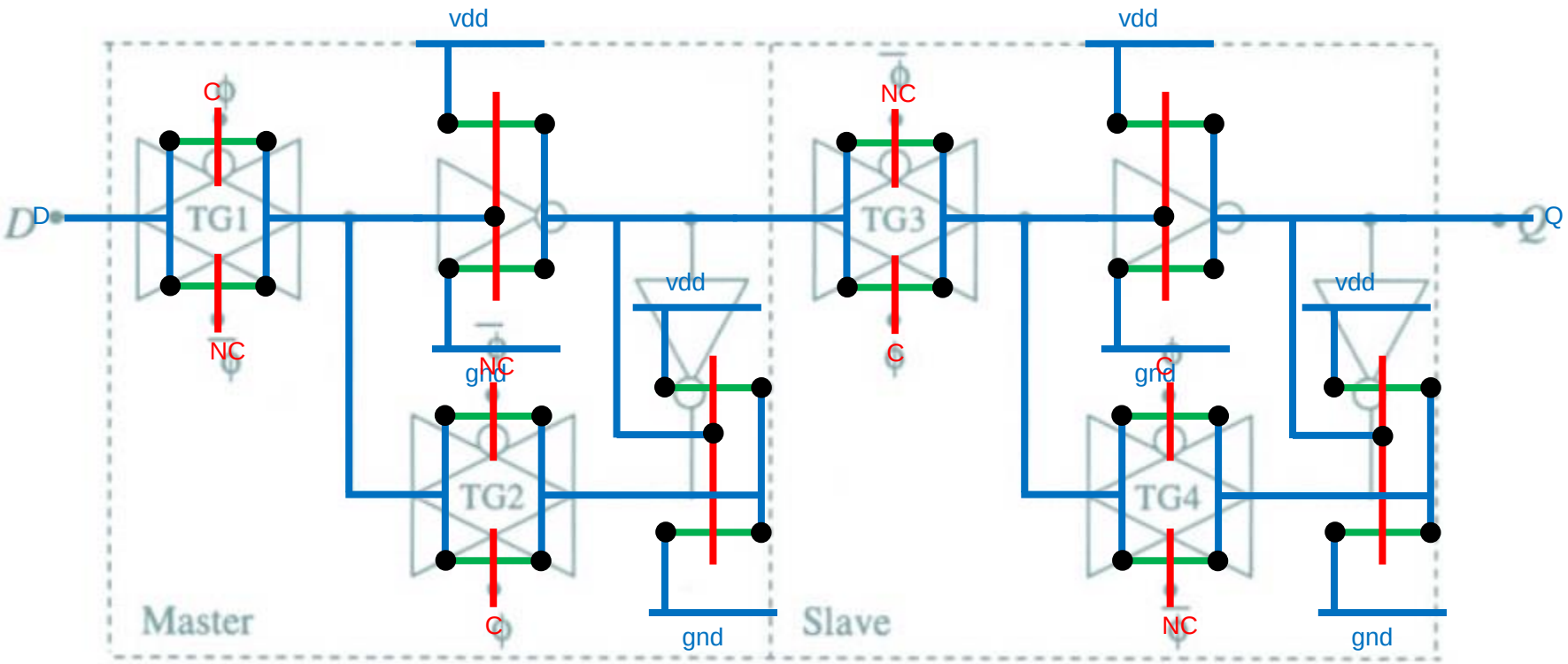
# D flip-flop

schematic → layout



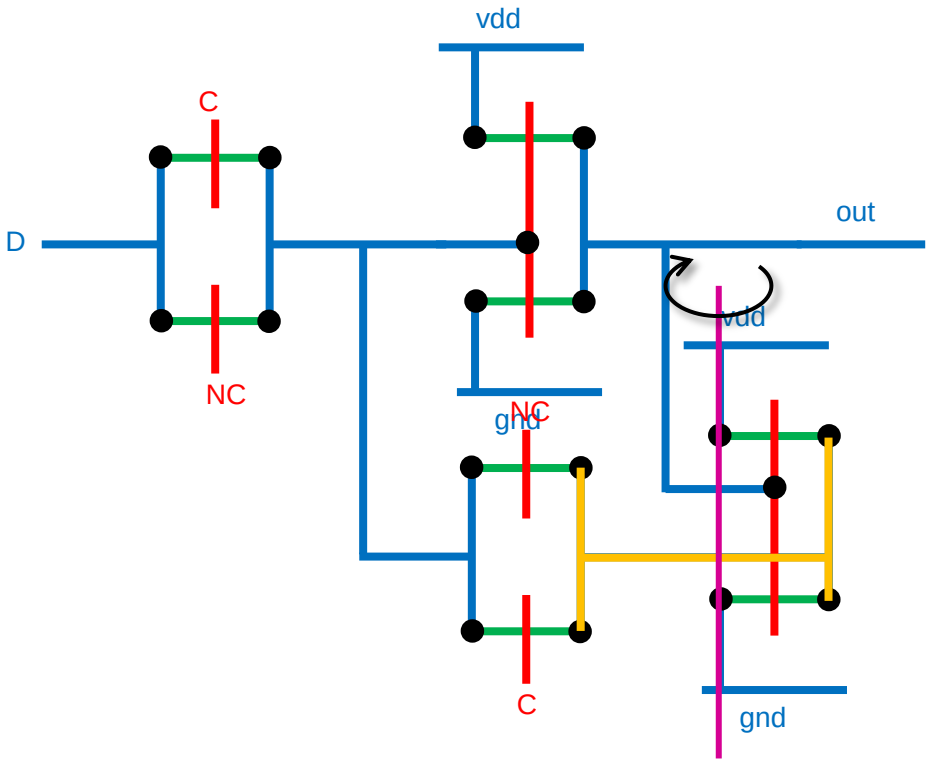
# D flip-flop

schematic → layout



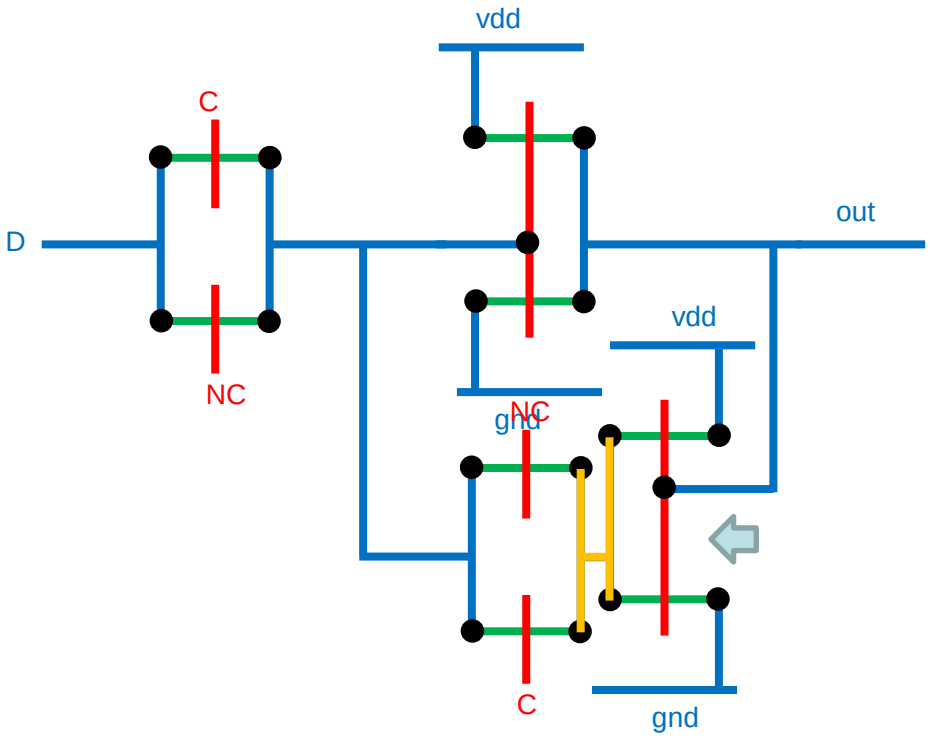
# D flip-flop

## The layout optimisation (1st latch)



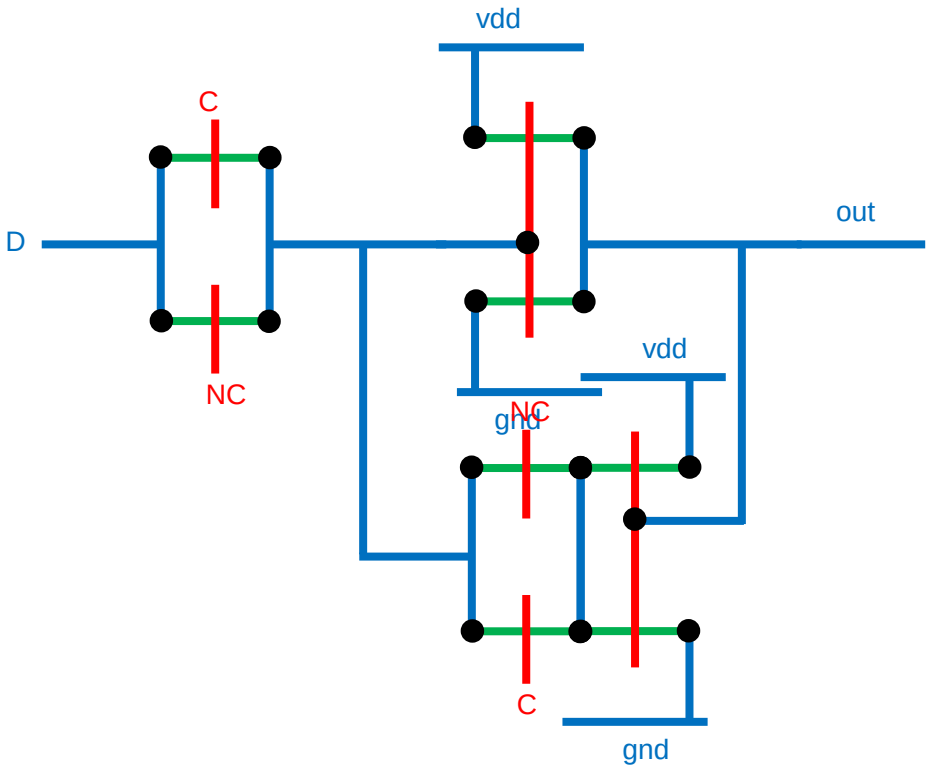
# D flip-flop

## The layout optimisation (1st latch)



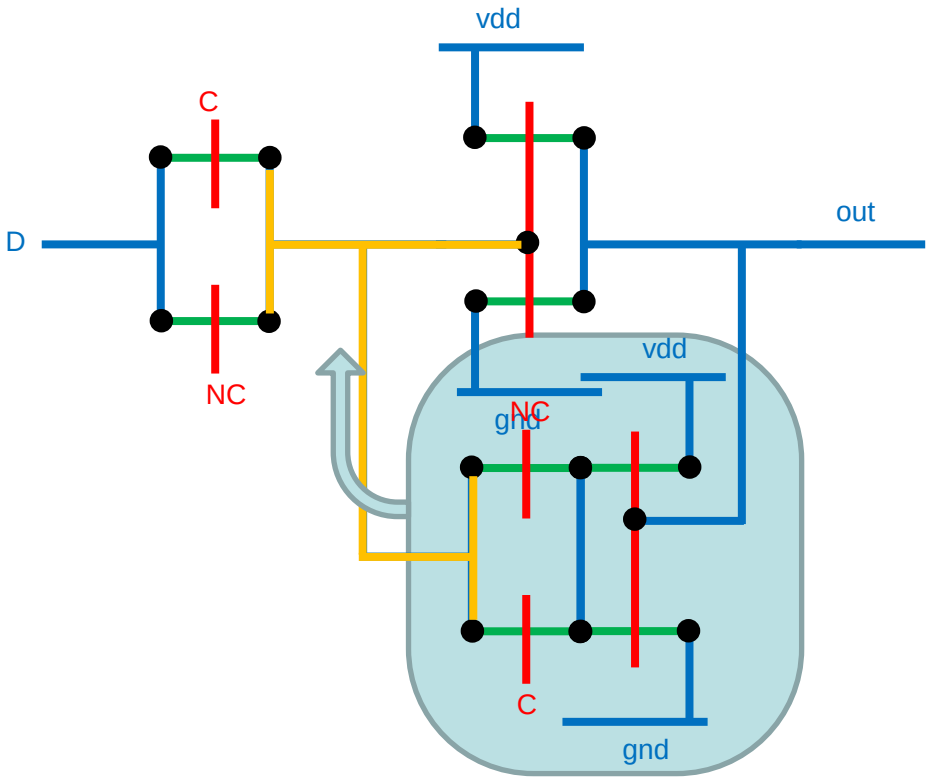
# D flip-flop

## The layout optimisation (1st latch)



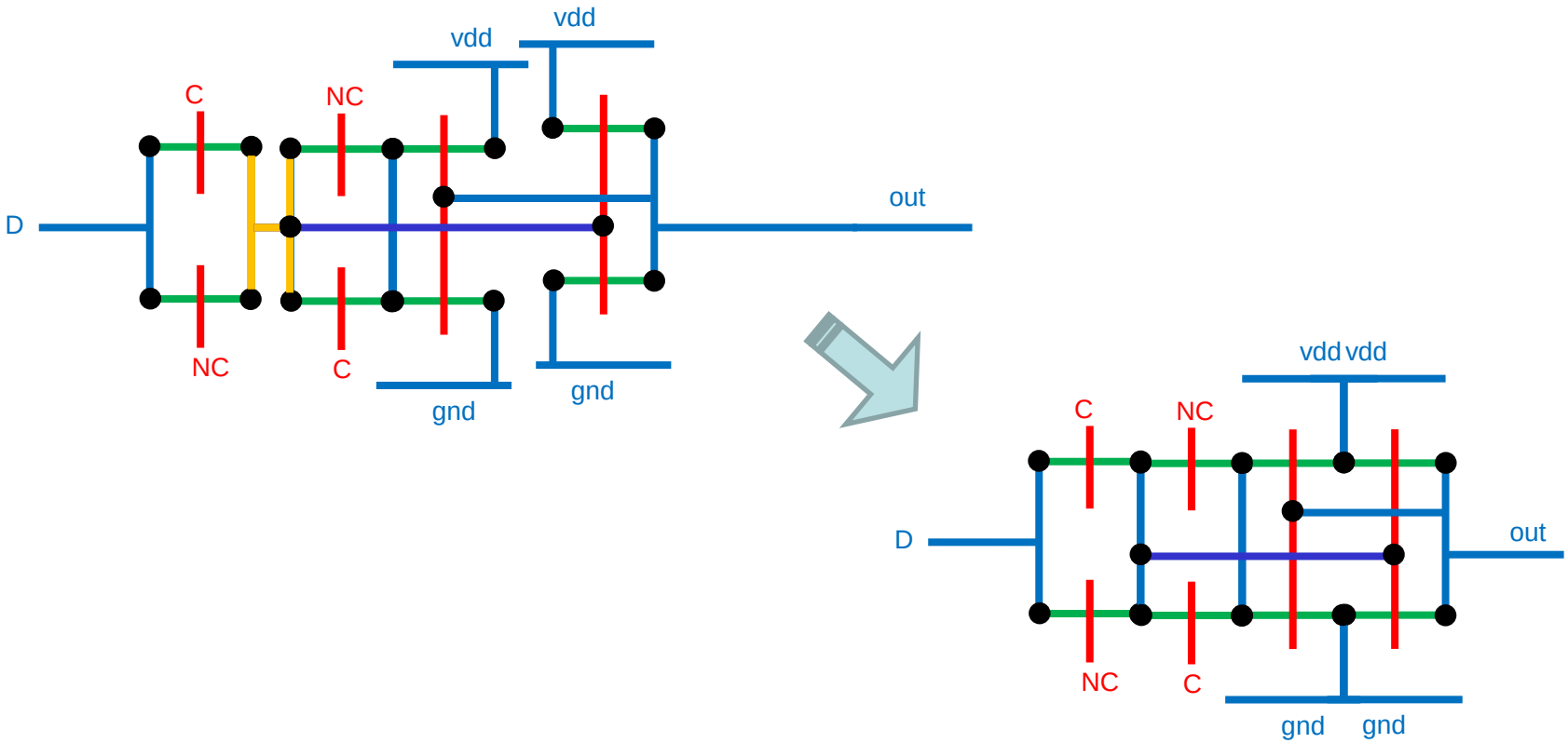
# D flip-flop

## The layout optimisation (1st latch)



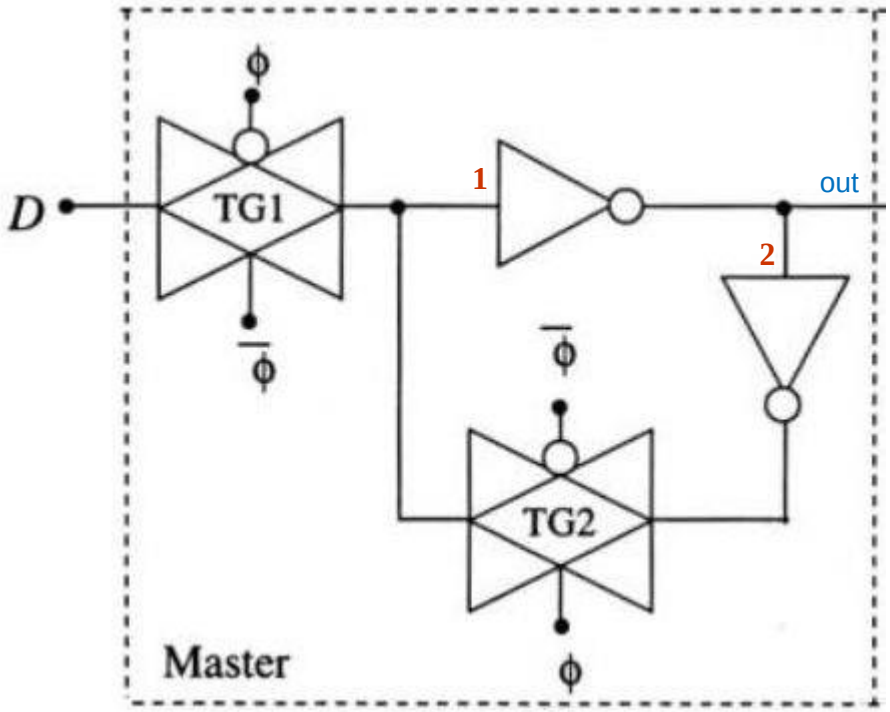
# D flip-flop

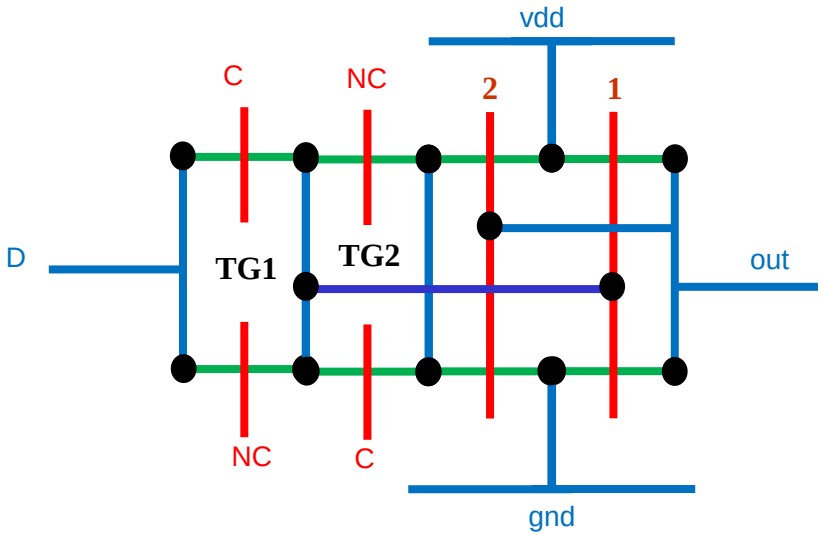
## The layout optimisation (1st latch)



# D flip-flop

The layout (1st latch) – comparison with the schematic



# D flip-flop

## The optimised layout