Laboratory of Integrated Systems Design

Department of Electronics

AGH University of Science and Technology in Cracow

Task 2
Design of NAND or NOR gate
optimisation of timing parameters

1. Purpose

Familiarizing students with the work of basic CMOS gates. Understanding the impact of the dimensions of transistors on a gate timing parameters. Acquiring skills to perform parametric simulations. Semi-automatic generation of a layout.

2. Task

- Draw a schematic diagram of the two-input NAND or NOR gate with minimum size transistors or take the schematic from task 1 (symmetrical gate). Perform a simulation confirming the correct work of the gate (e.g. transient analysis).
- Simulate serially connected 10 gates in order to determine the characteristic times of the gate (these are the times of propagation: t_{pHL} and t_{pLH}, and the rise and fall of the output signal in certain conditions). Consider two cases of setting the rise and fall times of the input signals: (a) very small values (e.g. 1 ps), (b) large values (e.g. 10 ns). Determine the propagation times and durations of the edges for each gate in the chain.
- Using the parametric analysis, choose the dimensions of transistors (width) to obtain gate time parameters as close as possible to previously determined characteristic times for given load of the gate. The load will be a multiple of the inverter's minimum input capacitance (assume that the inverter's input capacitance is 3fF).
- Draw a layout using the semi-automatic method. Keep the smallest dimensions of the layers and the space between them (possibly expand those layers that you need but do not increase the dimensions of the whole gate, e.g. power lines).
- Extract the netlist from the layout with parasitic parameters: R and C. Perform post-layout simulations to determine voltage-transfer characteristics and time parameters (propagation time, rise and fall time of the output signal) and average power consumption when loading the gate with a capacitance of 10 fF.

3. Result

- Present the final layout to check by the teacher.
- Write a short report containing: aim of the project and the results of pre-layout and post-layout simulations, i.e. obtained gate parameters: timing parameters: delay and rising, falling times, average power consumption, dimensions and area. Please remember to give the conditions the gate simulations (load capacitance, signal frequency, etc.). It is not advisable to place the topography in the report, but it is necessary to specify the path and name of the library where the final version of the project exist in your account. The report can be sent by e-mail, entering the subject of the letter: ICS_task2_name_surname.

4. Realization of the task – useful information

During this task, you can use information on parametric simulations and semi-automatic layout generation contained in the instructions for task 1.