Laboratory of Integrated Systems Design

Department of Electronics

AGH University of Science and Technology in Cracow

Task 4

Design of D flip-flop

layout optimisation

1. Purpose

Familiarizing students with the work of D flip-flop built of transmission gates in CMOS technology. Optimisation of a layout and minimisation of occupied area.

2. Task

- Draw a schematic diagram of the D flip-flop built of transmission gates. Perform a simulation confirming the correct work of the flip-flop (e.g. transient analysis).
- Draw the layout of the D flip-flop in such a way that all PMOS and NMOS transistors should be placed on one strip of P^+ and N^+ layer respectively. Keep the dimensions of the layers as small as possible and also the spacing (optionally extend these layers that are needed, but do not increase dimensions of the cell, e.g. supply lines should be as wide as possible).
- Extract the netlist from the layout with parasitic parameters: R and C. Perform post-layout simulations to determine time parameters (propagation time, rise and fall time of the output signal) and average power consumption when loading the flip-flop with a capacitance of 10 fF.

3. Result

- Present the final layout to check by the teacher.
- Write a short report containing: aim of the project and the results of post-layout simulations – parameters of the flip-flop: delay and edges times, average power consumption, dimensions and area. Please remember to give the conditions the flip-flop simulations (load capacitance, signal frequency, etc.). It is not advisable to place the topography in the report, but it is necessary to specify the path and name of the library where the final version of the project exist in your account. The report can be sent by e-mail, entering the subject of the letter: ICS_task4_name_surname.

4. Realization of the task – useful information

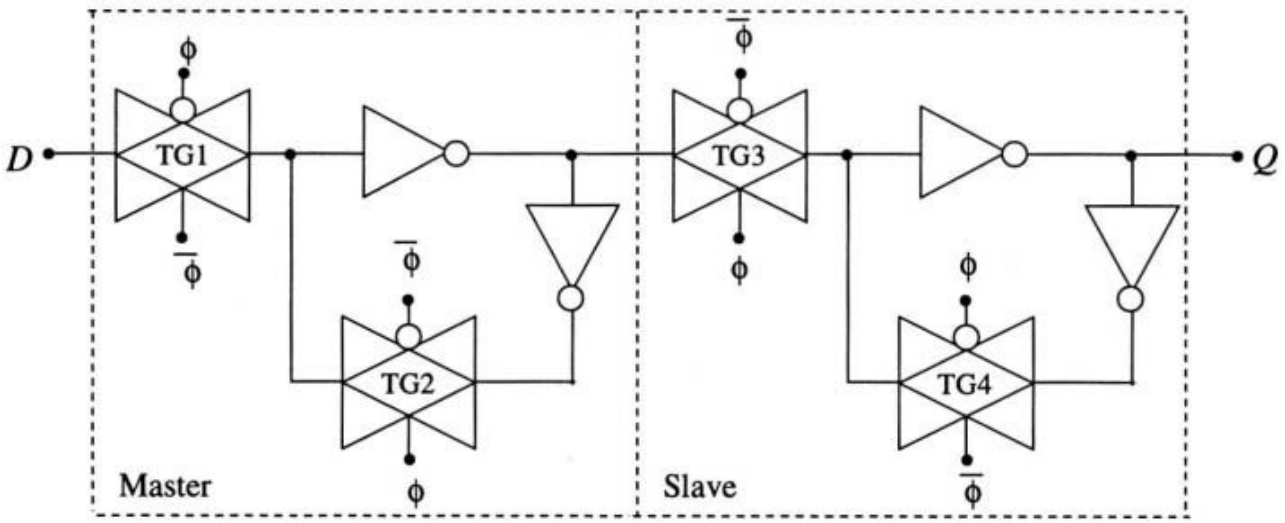
4.1. Initial settings and the gate schematic diagram

Recommendations such as in the previous task – you can create a new directory for the task or you can work in the existing design directory. But necessarily create a new library when you use later case. The schematic of the flip-flop can be drawn in two ways: using only transistors or using inverters and transmission gates. In the second case, the needed gates (schematics and symbols only) have to be prepared firstly.

4.2. The layout optimisation

Initially, layout elements can be generated from the schematic (similarly as in Task 1). Next, transistors have to be placed in such a way, that transistors of the same type are connected together resulting in one strip of the N^+ layer (for NMOS) and the second strip of the P^+ layer for PMOS's. You can utilise the method of complex gates design (transistors placement optimisation) described in instruction for Task 2.

4.3. Schematic the D flip-flop



The figure from: John P. Uyemura „CMOS logic circuit design”, Kluwer 2002