Laboratory of Integrated Systems Design

Department of Electronics

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Task 6

Design of a buffer with large load

transistors with big dimensions

1. Purpose

Familiarizing students with designing of have load buffer and calculations. Optimisation of a layout with big dimensions transistors (multi-finger transistors).

2. Task

- Perform simulations and measure propagation times (t_{pHL}, t_{pLH}) for a symmetrical inverter (see section 4.1) with the minimum dimensions for the load capacitance chosen from Tab. 1.
- Based on the theory [1] calculate number of the buffer stages (*N*) and size factor (*A*) assuming input capacitance C_{IN} = 3,5fF.
- Draw a circuit diagram for the above mensioned calculations. Perform a simulation confirming the correct work of the buffer and measure the its propagation times. Check how the increase in the size factor *A* (and the decrease in the number of stages *N*) will affect the propagation times. You can try to increase *A* one and a half times or twice.
- Draw a buffer layout using multi-finger transistors. Choose the size of the fingers so that the transistor "heights" are the same and they could be easy connected together. Pay attention to minimizing the area of the layout.
- Extract the netlist from the layout with parasitic parameters: R and C. Perform post-layout simulations to measure timing parameters (propagation times, rise and fall times) when loading the buffer with given capacitance. And measure average power consumption of the buffer without load.

3. Result

- Present the final layout to check by the teacher.
- Write a short report containing: the goal of the project and the results of pre-layout and post-layout simulations – compare times values when the given capacitance is driven by minimum inverter and the designed buffer. Collect (in a table) parameters of the buffer: i.e.: timing parameters, average power consumption, dimensions and area. Please remember to give the conditions the gate simulations (load capacitance, signal frequency, etc.). It is not advisable to place the topography in the report, but it is necessary to specify the path and name of the library where the final version of the project exist in your account. The report can be sent by e-mail, entering the subject of the letter: ICS_task6_name_surname.

Table 1. Load capacitance values for the buffor [pF].

L.p.	1	2	3	4	5	6	7	8
C_{load}	0.2	0.5	1	3	5	10	25	50

4. References

1. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 3rd Edition, October 2010, Wiley-IEEE Press, pp. 344 - 346.

5. Realization of the task – useful information

5.1. Schematic

The goal of the project is to minimize propagation times, thus, the minimum dimensions of transistors in the inverter for which we obtain the same propagation times t_{pLH} and t_{pHL} are: WP = 720 nm and WN = 240 nm with the length L = 180 nm (Task 1). The input capacity of such an inverter is approx. 3fF.

Drawing the schematic you should choose the size of fingers of the transistors in such way that, in subsequent stages (transistors) it is the same, and increase only the number of fingers to obtain assumed total width of the transistor. When drawing the schematic, enter the total width and number of fingers or finger dimension for each transistor, and the program will calculate the number of fingers (see Fig.1 below).

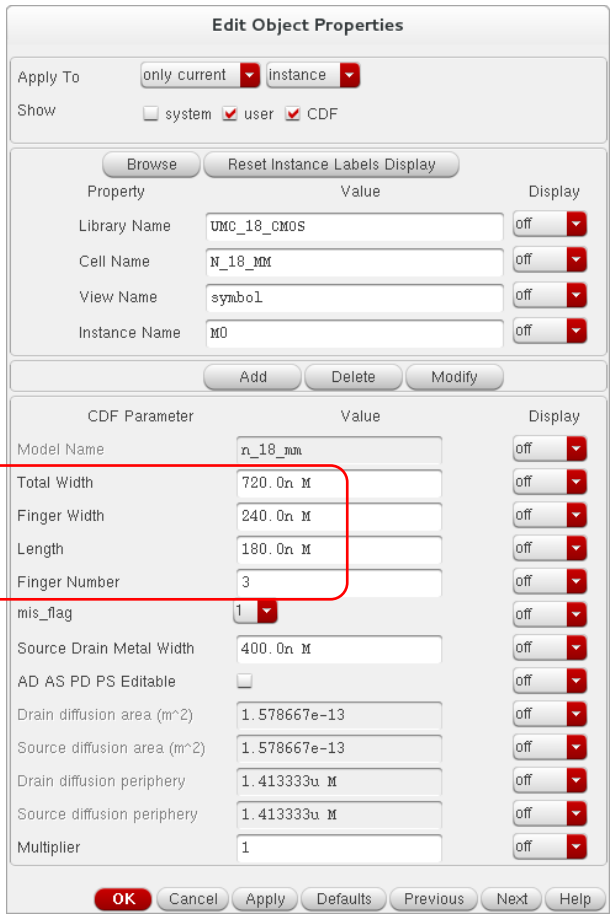

Fig. 1. Window for editing of a transistor parameters

5.1. Layout

The best way is to generate the layout automatically, next arrange transistors and connect them. Since the fingers of all transistors should to have the same dimension, the transistors visible on the topography will have the same vertical dimension and different horizontal, so they can be arranged side by side. All you need to do is connect the drains, sources and gates.

Below, in Figure 2, exemplary layout of transistors with identical finger sizes are shown. As you can see, the multi-finger transistor consists of several transistors that can be connected in parallel.

On one of them, metal layers have been marked, which have to be connected in order to create a drain and source of the transistor. The polysilicon strips should also be drawn to crate the gate.

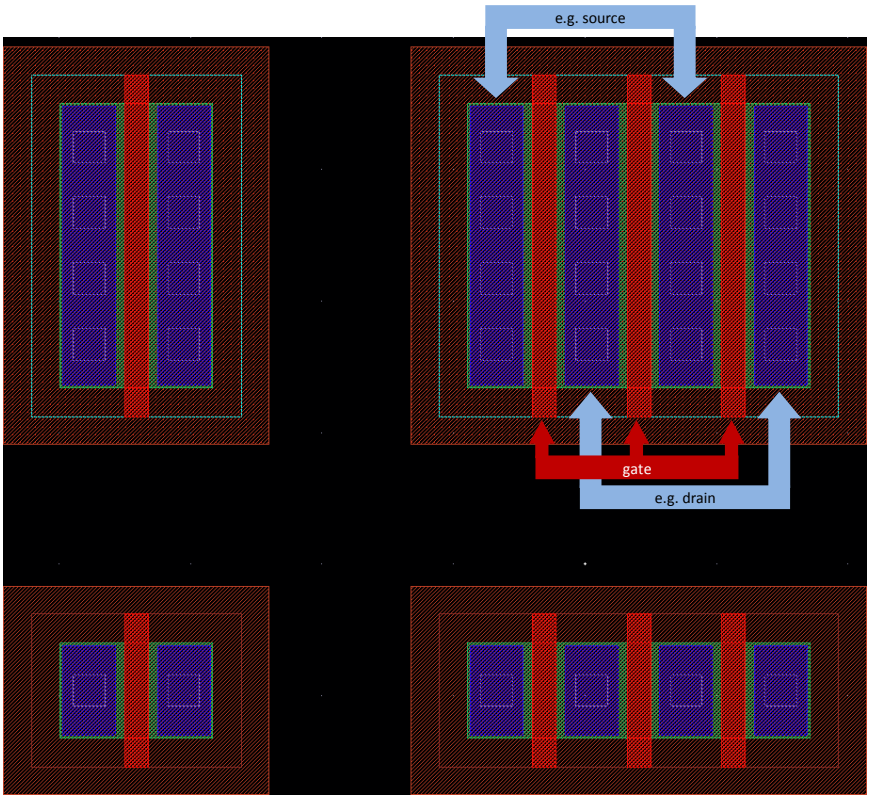

Fig. 2. Exemplary layouts of multi-finger transistors

Drawing the layout parameters of a transistor can be modified (Fig. 3).

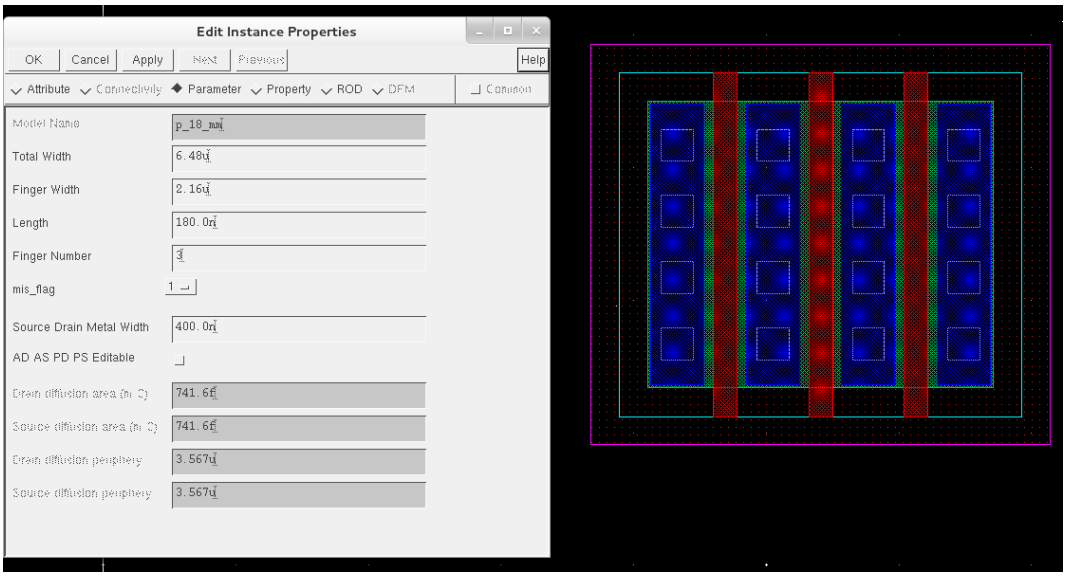

Fig. 3. Window for editing of transistor parameters in Virtuoso Layout Editor