Digital ASIC Design

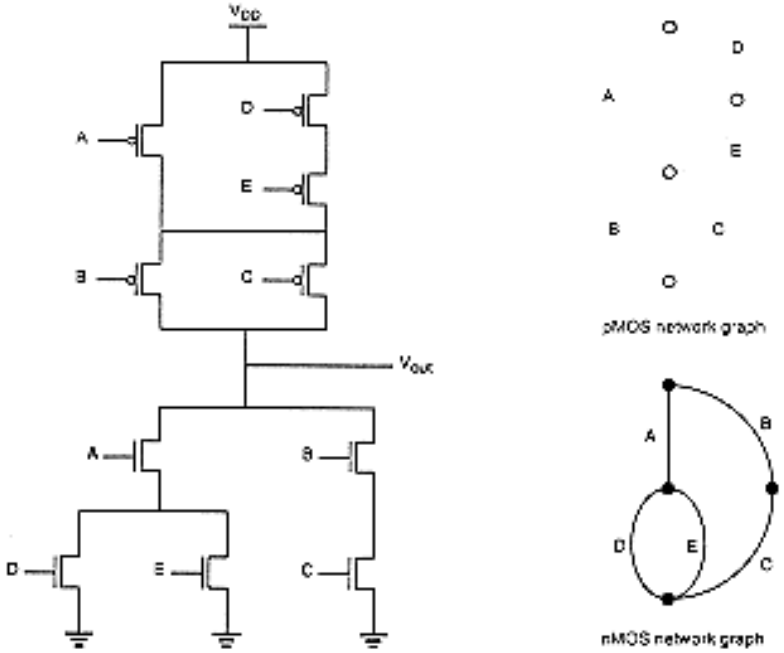
Task 2. D flip-flop, economic layout design.

Your second task is to draw a layout of a D flip-flip in a specific way. Please complete following steps:

- Draw a schematic of your D flip-flop. Use default transistors.
- Make transient analysis to find out if it works.
- Design your layout so that all of transistors PMOS and NMOS will be respectively connected by diffusion.
- Make standard DRC and LVS.

How to optimize a layout?

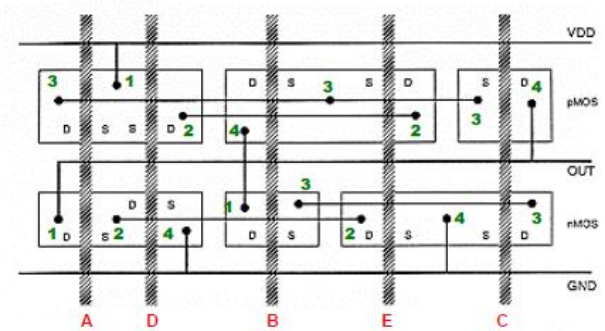
Let's consider a complex gate that realizes following logic function:
$f = \overline{A \cdot (B + C) + D \cdot E}$ (irrelevant for this task).



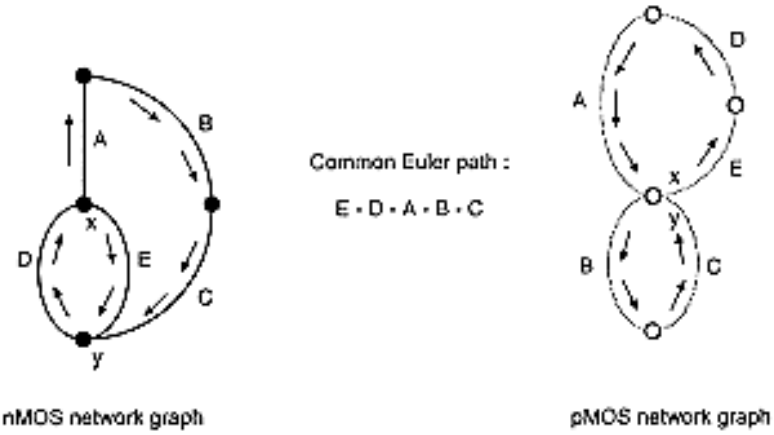
pMOS network graph

nMOS network graph

First step is to arbitrary select topological order of polysilicon gates, shown below. In this case a layout area have to be this large to fit two separations of diffusions.

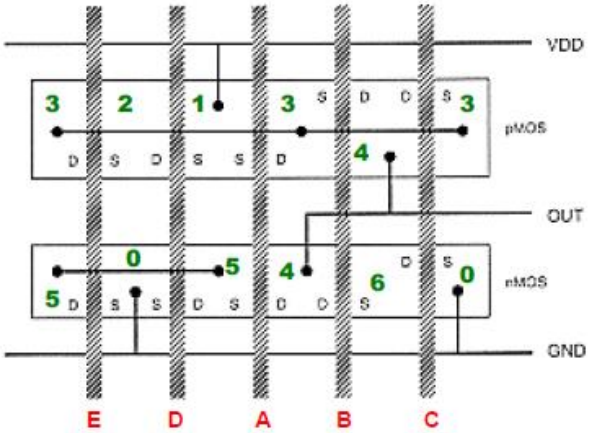


In order to make your layout more area efficient we make use of Euler method to find optimal path. We make two graphs for NMOS and PMOS nets with the same order of inputs. Now we are looking the same path, that goes through all nodes only once.



nMOS network graph pMOS network graph

We have chosen path E-D-A-B-C in both graphs.



Unfortunately mostly it isn't possible to find Euler path that goes through whole circuit. Best approach is to find longest path possible.

Suggested D flip-flop schematic