

EXCESS

A Flexible IC Circuit Extractor

User's Manual

Version 3.1 for Apple Macintosh computers

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Table of contents

1	Preface	1-1	
1.1	What is EXCESS?	1-2	
1.2	Hardware and software necessary for running EXCESS	1-2	
1.3	Setting up EXCESS		
2	First Session	2-1	
3	Extraction Mode Reference	3-1	
3.1	Working with EXCESS in Extraction Mode	3-1	
3.1.1	Manipulating technologies in Extraction Mode	3-1	
3.1.2	Manipulating layouts	3-2	
3.1.3	Setting the subset of components to be extracted	3–5	
3.1.4	Extraction of the electrical circuit	3-6	
3.2	Using menus in Extraction Mode	3-9	
3.2.1	Apple menu	3-9	
3.2.2	File menu	3-9	
3.2.6	Run menu		
3.2.7	Current technology menu		
3.2.7	Layout menu		
4	Technology Edit Mode Reference	4-1	
4.1	Working with EXCESS in Technology Edit Mode	4-3	
4.1.1	Manipulating technologies in Technology Edit Mode	4-3	
4.1.2	Defining masks	4-4	
4.1.3	Defining layers		
4.1.4	Defining composite devices		
4.1.5	Defining device sets		
4.1.6	Defining the standard network extraction options	4-14	
Appendix	A CIF file format	App-1	
Appendix	Appendix B Known bugs and problems		

1. Preface

This manual is an introduction to the integrated circuit layout extractor called EXCESS. EXCESS is one of the CAD tools in the IMiOCAD toolset - a set of programs for integrated circuit design, verification and simulation developed at Warsaw University of Technology, Warsaw, Poland. The manual describes the version of EXCESS for Apple Macintosh personal computers and assumes that you are familiar with Macintosh and MacOS operating system. If you never used Macintosh computers, please consult the Macintosh manual.

In addition, this manual assumes that you are familiar with the basics of VLSI design, in particular with masks that are used in IC technologies. A working knowledge of technological processes used in IC manufacturing is necessary for creating new technology descriptions for EXCESS. The "Atlas of IC technologies" by W. Maly is an excellent source of basic knowledge about technological processes used in the semiconductor industry.

The user of this manual should also be familiar with the Caltech Intermediate Format (CIF) layout description language and SPICE electrical simulator.

This manual is organized in three chapters. The First Session guides you through the basics of EXCESS operation while you extract the electrical circuit from a simple gate layout. The Extraction Mode Reference presents the basic principles of EXCESS implementation as a circuit extractor. The remaining chapter Technology Edit Mode Reference is a reference manual concerned with the technology definition mode. The technologies supplied with EXCESS are described in appendices.

The operation of EXCESS is quite simple. It is suggested that you proceed as follows:

- Read the rest of the Preface. It tells you how to set up EXCESS.
- Start up EXCESS on your Macintosh and perform the activities described in the First Session chapter. This should give you the basic grasp of EXCESS operation.
- Read the Extraction Mode Reference chapter. It explains some of the ideas of EXCESS in details.

At this point, if you do not want to get too deeply involved with EXCESS, you can read only the descriptions of the technologies you will use. After that, you should be able to work with your integrated circuit layouts right away.

If you want to work with a layout designed in a technology that is not supplied with EXCESS, or if you want to change the definition of some of the supplied technologies, you will have to acquaint yourself with technology editing. In this case, it is suggested that you proceed as follows:

- Read the Technology Edit Mode Reference.
- Read the description of the n-scmos technology.
- Run EXCESS in the Technology Edit Mode and look at the technologies supplied with EXCESS.
- Try to edit your own technologies.

The following conventions are used throughout this manual:

- Names of files and folders are printed in Helvetica font.
- Names of items in menus and dialogs are printed in Chicago font, just as they appear on the Macintosh screen.

1.1 What is EXCESS?

EXCESS is a circuit extractor: a computer program that can be used to extract electrical circuits directly from layouts of integrated circuits. Some of its features are:

- user defined technology,
- user defined subset of extracted devices,
- Caltech Intermediate Format (CIF) data input,
- SPICE format data output.

The unique feature of EXCESS is its graphical display of components that have been extracted. It is possible to locate the extracted components within the mask artwork displayed on the screen.

1.2 Hardware and software necessary for running EXCESS

EXCESS requires a Macintosh computer with at least two megabytes of memory. There are three versions of EXCESS. EXCESS version 3.1ppc is a PowerPC native code application running on any Power Macintosh. EXCESS version 3.1 runs on Macintoshes with Motorola 68020, 68030 or 68040 processor and a floating point coprocessor. EXCESS version 3.1nc runs on any Macintosh computer (with the exception of the two oldest models: Macintosh 128k and Macintosh 512k).

EXCESS may not run correctly with obsolete versions of the Macintosh system software. At the time of writing this manual the most recent release of the Macintosh system software was MacOS 7.5.5.

1.3 Setting up EXCESS

IMPORTANT: FIRST OF ALL, MAKE A BAKUP COPY OF THE EXCESS DISK.

The master disk supplied with this manual should be stored safely, away from any heat or magnetic field sources, so that it is possible to make another copy in case something happens to the working copy.

On the EXCESS distribution disk you may find either two folders: the EXCESS Folder and the Samples Folder, or the EXCESS Installer. Installation procedure for EXCESS is very simple. All you need to do is to copy the entire EXCESS Folder to your hard disk. If you have a disk with the EXCESS Installer, the Installer will do the job for you. Just open the Installer application and follow the instructions on the screen. Remember that the version of EXCESS you install (EXCESS 3.1, EXCESS 3.1ppc or EXCESS 3.1nc) must correspond to the type of processor in your Macintosh. The installer will ask you to indicate folder in which EXCESS folders are to be placed. Once the program file and other files are installed, you may start using EXCESS. The Samples Folder contains several IC layouts and circuit description files; there is no need to copy it to the working disk.

The EXCESS Folder contains the following files:



- this is the application itself. There are three versions: for 68k Macintosh without floating point coprocessor, for 68k Macintosh equipped with floating point coprocessor and for Power Macintosh.



- these are files with technology descriptions.

In addition to the kinds of files listed above, EXCESS also uses and maintains the *preference file* named EXCESS Prefs. This file is created automatically when you start up EXCESS for the first time after installation. The preference file is placed either in the System Folder or in the special folder named Preferences in the System Folder, depending on the version of the Macitnosh system software. The preference file is a place where your settings customizing operation of EXCESS are stored. It also keeps track of the default technology file.

2 First Session

This chapter will lead you through an example of a NAND gate circuit in the n-well CMOS technology. The variant of the CMOS technology you will be using is called n-SCMOS. It is a generic 1 micrometer CMOS technology based on the public domain MOSIS scmos technology.

• Start up EXCESS by double clicking its icon.

A startup dialog will appear:



Then a menu bar will appear with only the Apple, File, Edit and Options menus active.

👹 File Edit Options Diew Bus

• Choose the **Open technology** command from the **File** menu. This tells EXCESS that you want to start working using a particular technology definition. A dialog box will be displayed asking you to enter the name of the file with this technology definition.

File	
Open Layou1	
Open Technology _K	ж0
New Technology 🤻	
Dutput	
Quit	жQ

• Locate the n-SCMOS.exc file, choose it and click the **OK** button.

EXCESS will display a new menu $n\-\SCMOS.exc$ to inform you which technology is currently used.

🕼 File Edit Options 🕬 🕬 Russ n-SCMOS.exc

• Choose the **n-SCMOS.exc** menu.

As menu items you can see the list of names of the device sets that can be extracted. These sets have been predefined in the technology file. You can work with any of these sets or you can define your own set.

The set **full** contains all possible components that can be extracted in the current technology. The set **nominal** can be used to extract MOS transistors only. Working with the **optimal** set means that you want to extract all the most important devices - both nominal and parasitic.

• Choose the **nominal** command from the **n-SCMOS.exc** menu.

A checkmark indicates that the **nominal** set has been selected.



n-SCM0S.exc	
Select Devices	
√ full	
nominal 🔨	
optimal 🦄	

Choose the **Open Layout** command from the **File** menu.
 This tells EXCESS that you want to start working with a IC layout. A dialog box will be displayed asking you to enter the name of the layout file.

File Ope	n Layout 🚬	
Clo Edi	se Technology t Technology	% 0
001	put	
Qui	t	жQ

- Remark: in the dialog you will see an additional pop-up menu with the names of several file formats. In the current implementation of EXCESS only the CIF format is available, other formats will be implemented in the future versions.
- Possible problem: only the names of the text files with the ".cif" extension will be displayed in the file selection dialog. Always remember to add the ".cif" extension to your CIF layout files, otherwise EXCESS will not be able to recognize and open them.
- Locate the "aoi.cif" file, choose it and click the **OK** button.

EXCESS will open a new window displaying the selected layout. The outlines of all masks will be shown. You will also notice several black dots with numbers and texts in parentheses, These are labels assigned by the designer to some specific points or areas of the masks such as inouts, outputs, supply voltage etc.



A new **Layout** menu item will also be shown in the menu bar.

🐞 File Edit Options View Run n-SCMOS.exc Layout

Choose the Layout menu.

As menu items you can see the list of masks that are used in the n-scmos technology. Every mask name is checked. This means that all of them are displayed on the screen.

Layout
Show All Masks
Hide All Masks
Hide Labels
√ nwell
✓ active
🗸 polysilicon
✓ cut_active
✓ cut_poly
✓ pselect
🗸 nselect
√ metal_1
🗸 via
✓ metal_2
√ glass
🗸 pad
✓ all_others

Choose the **Hide All Masks** command from the **Layout** menu.

Your layout is no longer visible. You can toggle visibility of any of the masks on and off by choosing its name from the **Layout** menu. As an example do this with metal_1 mask.



The metal_1 mask becomes visible. Choose other masks - you can see any combination of them.



- Choose the Show All Masks command from the Layout menu. All masks become visible again.
- Notice that there are five labels assied to gnpaths on the aoi cell layout: power supply (vdd), ground (gnd) and three inputs (a, b, c). There is no "output" label. Click any point on the output signal path to create the label.



The window for adding labels will appear:



Enter the name of the label (label text) and the number that you want to assign to it (do not use any of the numbers already assigned) and click the **OK** button. The new label will appear in the layout window.

aoi.cif

• Choose the **Turn Grid On** command from the **View** menu.

After you chose the **Turn Grid On** command, the layout area has become filled with equally spaced dots. The distance between adjacent dots is 1.5 micrometer. You can change this distance by choosing the **Grid Scale...** command from the **Uiew** menu. The grid helps to determine the dimensions of the mask features.

- Choose the **Zoom In** command from the **Uiew** menu.
 The layout drawing becomes enlarged twice. (It is possible to obtain the same effect by clicking the *zoom icon* in the lower left corner of the layout window).
- Choose the Zoom Out command from the Uiew menu.
 The layout drawing becomes reduced twice. (It is possible to obtain the same effect by pressing the OPTION key and clicking the zoom icon).

Now you can start the extraction process.

• Choose the **Circuit Extraction** command from the **Run** menu. EXCESS will analyze your layout and search all components from the selected device set. The progress of the extraction process is shown in the progress bar window. When the extraction is completed, this window disappears.







Choose the **n**-**SCMOS.exc** menu. •

Note that the items in this menu have changed. Now the menu displays a list of names of devices that have been extracted. Since you have chosen the **nominal** extraction set, only two kinds of devices have been extracted from the layout. Both of them are transistors: p-channel MOS transistors and n-channel MOS transistors.

Choose the Mos trans.: Nchan from n-SCMOS.exc menu.

All channels of n-channel transistors have become highlighted with light grey color (or pattern in black and white mode). You can observe the positions of these transistors within your layout. In the same manner you can highlight p-channel transistors and observe them.

Choose the **Output** command from the **File** menu.

aoi.cir

This tells EXCESS that you want to calculate electric parameters of each extracted component and create a circuit file in Spice format. A standard Macintosh dialog box will be displayed asking you to enter the name of the output file. The default name is the layout CIF file name with the extension ".cif" replaced by ".cir".

Leave the default name and click the save button. The progress bar showing the progress in calculations of device parameters is displayed. When the calculations are completed the progress bar window disappears.

Open the output "aoi.cir" file using your favorite text editor. EXCESS output files are text files readable by all Macintosh text editors. The contents of the file is shown below.

> *Node numbers: _ Labels: * (assigned to Metal1) 1 out * 2 (assigned to Metall) _ а * 3 _ (assigned to Metall) b * 4 (assigned to Metal1) С * 0 (assigned to Metall) (ov) _ gnd (assigned to Metall) 6 vdd

n-SCMOS.exc Mos trans.: Pchan Mos trans.: Nchan

n-SCM0S.exc Mos trans.: Pchan Mos trans,: Nchan







```
*Circuit netlist:
          6276
                   Pchan W=1.5E-05 L=3E-06
M1Pchan
         7316
M2Pchan
                   Pchan W=1.5E-05 L=3E-06
                   Pchan W=1.5E-05 L=3E-06
         1476
M3Pchan
                   Nchan W=6E-06 L=3E-06
MlNchan
         1 2 0 0
M2Nchan
         0 3 8 0
                   Nchan W=6E-06 L=3E-06
M3Nchan
         8410
                   Nchan W=6E-06 L=3E-06
.MODEL Pchan PMOS
+ LEVEL=2 LD=0.03 TOX=2.25E-08 NSUB=6.57544E+16 VTO=-0.63025
+ KP=2.63544E-05 GAMMA=0.618101 PHI=0.541111 UO=361.941 UEXP=0.0888696
+ UCRIT=637449 DELTA=0 VMAX=63253.3 XJ=0.112799 LAMBDA=0
+ NFS=1.66844E+11 NEFF=0.64354 NSS=3E+10 TPG=-1 RSH=150
+ CGSO=3.35E-10 CGDO=3.35E-10 CJ=0.000475 MJ=0.341 CJSW=2.23E-10
+ MJSW=0.307
.MODEL Nchan NMOS
+ LEVEL=2 LD=0 TOX=2.25E-08 NSUB=1.066E+16 VTO=0.62249
+ KP=6.32664E-05 GAMMA=0.639243 PHI=0.31 UO=1215.74 UEXP=0.0461235
+ UCRIT=174667 DELTA=0 VMAX=177269 XJ=0.9 LAMBDA=0
+ NFS=4.55168E+12 NEFF=4.6883 NSS=3E+10 TPG=1 RSH=60
+ CGSO=2.89E-10 CGDO=2.89E-10 CJ=0.000327 MJ=1.067 CJSW=1.74E-10
+ MJSW=0.195
```

. END

You may notice that:

- labels that were placed in the layout are shown as Spice comments with node numbers assigned to them,

- the file contains the extracted netlist as well as device models, but no definition of supply voltages, input signals etc. and no Spice command lines.

To perform Spice simulation, you will have to add these lines yourself. Do not do this now. Leave the "aoi.cir" file opened and go back to EXCESS.

Choose the New Extraction command from the Run menu.
 This tells EXCESS that you want to start next extraction from the same layout.



Remark: to work with another layout, you should close current layout by clicking the window close box or by choosing the **Close Layout** command from the **File** menu, and open the new layout file.

• Choose the **Select devices...** command from the **n-SCMOS.exc** menu.

A dialog that allows you to create a custom list of device types to be extracted is displayed. It lists all types of components that can be created in the current technology. The name of the device set currently chosen from the **n-SCMOS.exc** menu is displayed in a text edit box, and the names of devices which belong to this set are highlighted. You may choose any set of the components by highlighting them. For example, choose both n-channel and p-channel transistors, all path resistances (metal, polysilicon, diffusion) and diodes: N-diffusion to substrate and P-diffusion to N-well. Such a set of components may be useful if you want to analyze the influence of parasitic components on the operation of your circuit. To select a device name on the list, press the COMMAND and SHIFT keys and click on an already selected and highlighted name. Once appropriate names of components are selected, click the **Add** button, enter a new set name (e.g. **my_set**) in the text edit box and click the **Select** button.

• Choose again the **Circuit Extraction** command from the **Run** menu. Once the extraction is completed, choose the the **n-SCMOS.exc** menu.

The list of device names which belong to **mu_set** appears in the menu. You may select these names, one at a time, in order to highlight the corresponding devices in the layout.

Choose the **Output** command from the **File** menu.

In the dialog that will appear change the default "aoi.cir" file name to something else, e.g. "my_aoi.cir", to avoid overwriting of the "aoi.cir" file created previously. Click the **Saue** button and wait until the new output Spice file is created. Open this file using your favourite text editor, and compare its contents with the contents of the "aoi.cir" file. Note that the new netlist is much longer, and includes metal, polysilicon and diffusion resistances. Don't be astonished by large number of extracted resistances. For every resistive area with more than two electrical terminals EXCESS assigns a network of resitors, not a single one.

my_aoi.cir *Node numbers: Labels: _ * 2 (assigned to Metall) а (assigned to Metall) * 3 _ b * 4 _ (assigned to Metall) С 0 (ov) - gnd (assigned to Metall) * _ (assigned to Metal1) 1 out _ 6 vdd (assigned to Metall) *Circuit netlist: R1RPoly 3 10 367.34 R2RPoly 39 268.371 R3RPoly 10 9 2107.27 4 11 208.609 R4RPoly R5RPoly 4 12 184.577 R6RPoly 2 13 385.401 R7RPoly 2 14 87.3629 R8RPoly 14 13 6000.68 15 16 R1RPdiff 72.3737 R2RPdiff 15 6 35.5799 R3RPdiff 86.5068 6 16 R4RPdiff 17 19 93.8253 17 18 R5RPdiff 150.849 R6RPdiff 17 7 34.2323 18 19 R7RPdiff 93.8253 R8RPdiff 18 7 34.2323 R9RPdiff 7 19 71.6242 R10RPdiff 20 22 93.8253 R11RPdiff 20 21 150.849 20 1 R12RPdiff 34,2323 R13RPdiff 21 22 93.8253 21 1 R14RPdiff 34.2323 R15RPdiff 1 22 71.6242 R16RPdiff 23 7 38.8235 R17RPdiff 23 24 60.2125 R18RPdiff 7 24 211.302 15 13 18 6 Pchan W=1.5E-05 L=3E-06 MlPchan 17 9 21 6 Pchan W=1.5E-05 L=3E-06 M2Pchan 20 11 23 6 M3Pchan Pchan W=1.5E-05 L=3E-06 403.756 R1RNdiff 25 26 25 1 R2RNdiff 30.8936 R3RNdiff 1 26 13.7535 R4RNdiff 27 28 403.756 R5RNdiff 27 0 30.8936 R6RNdiff 0 28 13.7535 29 30 R7RNdiff 403.756 R8RNdiff 29 0 30.8936 R9RNdiff 0 30 13.7535 R10RNdiff 31 33 46.8613 R11RNdiff 31 32 73.6777 R12RNdiff 32 33 46.8613 R13RNdiff 34 35 403.756 R14RNdiff 34 1 30.8936 R15RNdiff 1 35 13.7535 25 14 27 0 Nchan W=6E-06 L=3E-06 MlNchan

```
M2Nchan 29 10 32 0
                       Nchan W=6E-06 L=3E-06
          31 12 34 0
                        Nchan W=6E-06 L=3E-06
M3Nchan
DlDPdiffNwell 16 6 DPdiffNwell 1.08E-10
D2DPdiffNwell 19 6 DPdiffNwell 1.44E-10
D3DPdiffNwell 22 6 DPdiffNwell 1.44E-10
D4DPdiffNwell 24 6 DPdiffNwell 8.1E-11
D5DPdiffNwell 1 6 DPdiffNwell 9E-12
D6DPdiffNwell 7 6 DPdiffNwell 1.8E-11
D1DNdiffsub 0 26 DNdiffsub 5.4E-11
D2DNdiffsub 0 28 DNdiffsub 5.4E-11
D3DNdiffsub 0 30 DNdiffsub 5.4E-11
D4DNdiffsub 0 33 DNdiffsub 2.7E-11
D5DNdiffsub 0 35 DNdiffsub 5.4E-11
D6DNdiffsub 0 1 DNdiffsub 1.8E-11
.MODEL Pchan PMOS
+ LEVEL=2 LD=0.03 TOX=2.25E-08 NSUB=6.57544E+16 VTO=-0.63025
+ KP=2.63544E-05 GAMMA=0.618101 PHI=0.541111 UO=361.941 UEXP=0.0888696
+ UCRIT=637449 DELTA=0 VMAX=63253.3 XJ=0.112799 LAMBDA=0
+ NFS=1.66844E+11 NEFF=0.64354 NSS=3E+10 TPG=-1 RSH=150
+ CGSO=3.35E-10 CGDO=3.35E-10 CJ=0.000475 MJ=0.341 CJSW=2.23E-10
+ MJSW=0.307
.MODEL Nchan NMOS
+ LEVEL=2 LD=0 TOX=2.25E-08 NSUB=1.066E+16 VTO=0.62249
+ KP=6.32664E-05 GAMMA=0.639243 PHI=0.31 UO=1215.74 UEXP=0.0461235
+ UCRIT=174667 DELTA=0 VMAX=177269 XJ=0.9 LAMBDA=0
+ NFS=4.55168E+12 NEFF=4.6883 NSS=3E+10 TPG=1 RSH=60
+ CGSO=2.89E-10 CGDO=2.89E-10 CJ=0.000327 MJ=1.067 CJSW=1.74E-10
+ MJSW=0.195
.MODEL DPdiffNwell D
+ IS=2E-06 VT=2.2E-06
.MODEL DNdiffsub D
+ IS=2E-06 VT=2.2E-06
END
```

At this moment you are familiar with the basics of EXCESS. You can open the technology file and the layout file, you know how to select a device set appropriate for the circuit simulation you want to perform, you know how to perform the extraction and to create the output Spice file. Basically, this is all you need for routine work with EXCESS. The rest of this manual will explain in more detail the operation of EXCESS and will show you how to make your own technology files.

3 Extraction Mode Reference

This chapter describes the means provided by EXCESS for extracting a circuit from an IC layout. It first tells how EXCESS is started up in Extraction Mode, how to select a technology, how to select a layout and how the data files can be saved, and read in. Following the description of the input/output commands, the operation of EXCESS as a circuit extractor and various options of EXCESS are discussed. You are already familiar with some of this chapter's contents from the First Session.

3.1 Working with EXCESS in Extraction Mode

EXCESS starts up in Extraction Mode if it is opened alone.

To open EXCESS alone:

• Select the EXCESS icon in the Finder and then choose the Open command from the File menu.

After displaying an information dialog EXCESS will draw a menu bar and wait for your commands. If a *default technology* has been defined previously and EXCESS finds a file with the description of this technology, this technology is opened and the standard dialog box will be shown. It alows to open your layout file (see Section 3.1.2 Manipulating layouts in Extraction Mode).

Alternate methods that can be used instead of choosing Open.

- Type the **#0** key.
- Double-click the EXCESS icon.

3.1.1 Manipulating technologies in Extraction Mode

After starting up EXCESS, you may want to declare the technology you want to use. At any given point during EXCESS execution in Extraction Mode, the technology being used is called the *current technology*.

To set the current technology:

• Pull down the File menu and choose the **Open technology** command.

The standard file opening dialog will be displayed. Only EXCESS technology files will be listed in the file selection box. You can open the file that contains the technology you want to work with. The name of the current technology file will be displayed as a new menu within the Macintosh menu bar. After setting the current technology you can read the layout description file. It is not possible to open a layout file if no current technology is defined.

Note: The current technology can be made the default technology. EXCESS tries to read the default technology just after starting up and opens it automatically. To set a technology as the default technology, open it, pull down the **Options** menu and choose the **Save Extractor Settings** command. The name of the current technology file and its location in the Macintosh file system will be saved in the EXCESS preference file. File Open Layout Open Technology #0 New Technology Output Quit #Q



After a technology file has been declared as the default one, do not move it to another folder or delete it.

Possible messages:

While reading the technology input file it is possible to obtain "Problem with input file" message. It means that either the file does not contain valid technology description (this can

happen if you attempt to open a technology file created by an old version of EXCESS) or the default technology file could not be found on the disk.

To close the current technology:

• Choose the **Close Technology** command from the **File** menu. The current technology name will be removed from the menu bar. If there is any open layout file, it will be closed too and all layout information will be removed from the memory.

Note: Executing **Saue Extractor Settings** command after closing the current technology will result in saving "no default technology" information in the preference file. During the next execution EXCESS will not read automatically any technology.

To edit the current technology:

 Choose the Edit Technology command form the File menu. EXCESS enters Technology Edit Mode. Consult the Technology Edit Mode Reference chapter for further instructions. Edit Technology command is active only when a technology is opened and there is no layout that has been read in.

Warning: Do not attempt to edit an existing good technology file unless you are quite sure that you know what you want to do and how to do that. It is very easy to loose crucial information or even to destroy the technology file completely. Even if you are an experienced user of EXCESS, always make a backup copy of a technology file before editing it.

To create a new technology:

 Choose the New Technology command from the File menu. EXCESS enters Technology Edit Mode. Consult the Technology Edit Mode Reference chapter for further instructions. New Technology command replaces the Edit Technology command and is active only when no current technology is opened.

3.1.2 Manipulating layouts

After choosing a technology you may want to declare the layout you want to work with. At any given point during EXCESS execution in Extraction Mode, the layout being used is called the *current layout*.

To set the current layout:

• Choose the **Open layout** command from the **File** menu.

A standard dialog box will be displayed asking you to enter the name of the layout file. Only file names with the ".cif" or ".CIF" extension will be displayed. The layout will be placed in a new window. All masks will be drawn as color (or black in black and white mode) contour outlines. The **Layout** menu will be added to the menu bar. This menu will allow you to work with the layout drawing.

In the case of incorrect data in the layout input file the CIF interpretation error message will be displayed and the layout window will not be created. The message contains the line number and a short description of the error. You should use a

File Open Layout	
Close Technology Edit Technology	ж0
Dutput	
Quit	жQ

<mark>File</mark> Open Layout	
Open Technology New Technology _N	¥0
output	
Quit	жQ



File

Open Layout

Dutput Nuit

Close Technology

жQ

Edit Technology

text editor to correct the error or to create the CIF file again and try to open the file once more.

Note: It is impossible to work with more than one layout file simultaneously.

To close the current layout:

Choose the CloseLayout command from the File menu.
 A dialog asking you to confirm your decision to close the layout will be displayed. If you click the Yes button, the window that contains the layout drawing will be closed and the Layout menu will be removed from the menu bar.

File Close Layout	
Close Technology Edit Technology	жO
Dutput	
Quit	жQ

Alternate method of closing the layout: Click in the layout window close box.

To change drawing scale:

• Choose either the **Zoom In** or the **Zoom Out** commad from the **View** menu.

The layout drawing will be either enlarged or reduced approximately twice.

Alternative method: Drawing scale can be changed by clicking the Zoom icon in the lower left corner of the layout window. Normally the Zoom icon displays the + sign and clicking it is equivalent to selection of the **Zoom In** command. When the COMMAND key is pressed, the sign in the Zoom icon changes to – and clicking it is equivalent to selection of the **Zoom Out** command.

To fit the layout drawing in the layout window:

- Choose the Fit To Window command from the View menu.
- The drawing scale will be adjusted to the current window size. The new drawing scale will allow to fit the whole IC artwork inside the window.

To scroll the layout view:

• Use standard Macintosh scroll bars.

To change the layout window size:

• Use standard Macintosh window boxes: the grow box and/or the zoom box.

To turn the visibility of the layout grid on and off, and to change grid scale:

• Choose the **Turn Grid On** command from the **View** menu.

The layout area will become filled with equally spaced dots. The standard distance between the adjacent dots is technology specific and can be defined in the technology file (see Technology Edit Mode Reference). You can change this distance using a dialog box that will be displayed after

choosing the **Grid Scale...** command from the **View** menu.

- Note: Grid dots are drawn only when the distance between them is greater then two pixels in the current screen scale.
- To remove grid from the layout window choose the **Turn Grid Off** command from the **Uiew** menu.









To hide or show the entire mask artwork:

• Use Hide All Masks or Show All Masks commands from the Layout menu.

To hide or show a single mask:

Pull down the **Layout** menu and select the name of the mask. If the mask outline is invisible, it will be drawn on the screen and the mask name will become checked on the mask list in the **Layout** menu. If the mask outline is visible, it will be removed from the screen and the mask name will become unchecked. In this way you can toggle visibility of any of the masks.

Note that on color screens the mask names in the menu are displayed in colors corresponding to the colors of the mask outlines. These colors are defined in the technology file.

Hide Labels 🗸 nwell 🗸 active 🗸 polysilicon ✓ cut_active ✓ cut_poly 🗸 pselect 🗸 nselect √ metal_1 🗸 via ✓ metal_2 🗸 glass √ pad ✓ all_others Layout Show all masks Hide all masks Hide labels nwell active

Layout

Show All Masks <u>Hide All Masks</u>

yout menu.

To hide or show labels:

Choose the **Hide Labels** or **Show Labels** command from the **Layout** menu.

Labels are usually added to the layout in a layout editor and transferred to EXCESS in the layout description CIF files. In most cases they are used to indicate some specific electrical nodes in the layout (e.g. inputs, outputs, ground, power supply etc.). EXCESS assigns numbers to all labels, starting from 1. After extraction these numbers will become node numbers in the Spice netlist. EXCESS draws labels as black dots. Each label dot is accompanied by the label text and the node number assigned by EXCESS. The label text is meaningless for EXCESS, but it is transferred to the Spice output file together with the node number, as Spice comment. In this way readability of the Spice file is greatly improved.

If some labels are missing or there are no labels at all in the layout, they can be added to the layout before extraction. It is also possible to modify existing labels.

To add or modify labels:

To add a new label, move the arrow cursor to the point where you want to create it and click the mouse button. The dialog box will appear.

Enter label :	
Number : 1	Uelete this label
Name : unknown	Cancel OK

Enter a number and the desired name (text) of the new label and click the $\mathbf{0}$ K button. The new label will be added to the list of labels and will be shown on the screen.

Remark: It is impossible to add a new label with a number that is already assigned to another label. It is possible to add a new label with already existing label name, but this is not recommended. It is usually confusing to have two or more node numbers with the same name in the Spice file.

• To edit existing label or to remove it, position the tip of the arrow cursor in the label dot and click the mouse button. Use the dialog box that will appear to edit the label attributes or to delete it.



3.1.3 Setting the subset of components to be extracted

All classes of components that can be extracted: MOS transistors, diodes, resistors, and capacitors of all kinds are defined in EXCESS technology files. EXCESS allows to select any subset of these components. It is even possible to extract a circuit that contains components belonging to a single class (e.g. you can find all polysilicon paths within your layout artwork). At the other hand it is possible to obtain the circuit that contains components belonging to all classes that have been defined in the technology file.

Before starting extraction you should determine the subset of the classes of components to be extracted. Such a subset will be called *extraction device set*. There are three types of them:

1. Permanent device sets. These sets are defined in technology files (see Technology Edit Mode Reference). They appear in the technology menu and can be selected every time when the technology is used.

2. Default device sets. The default device set is a set that is selected automatically when the default technology is read in. The name of the default device set is stored in the EXCESS preference file.

3. Temporary device sets. These sets can be defined during current working session and can be used until the session ends or the current technology is closed. The temporary device sets are not stored in the technology file, but they can be saved for later use in the EXCESS preference file.

To select an existing extraction device set:

Pull down the current technology menu and choose the name of the device set you want to use.



To find out what classes of components belong to the selected device set:

• Select the set by choosing its name from the current technology menu, then choose the **Select Devices...** command from the same menu. A dialog that contains a list of all available classes of components will be displayed, and the components that belong to the selected class will be highlighted. Once you have learned what components belong to the selected device set, dismiss the dialog by clicking the **Cancel** button.

To define a temporary device set:

• Pull down the current technology menu and choose the **Select devices...** command. The dialog box that contains a list of all available components will be displayed.

You can define a new device extraction set by selecting all components that you want to work with. To add a class of components to the existing selection, press the COMMAND key and click on the name of this class. To deselect an already selected class of components, press the COMMAND key and click on the name of this class. When all desired components are highlighted, you have two options. If you click the **Select set** button and dismiss the dialog with the **OK** button, the set

of highlighted components will be selected for extraction, but no new set name will appear in the current technology menu. This option is useful only if you want to define a set for one time use. Another option is to click the **Add set** button in the **Custom device set** box and enter a name of the set in the **Set name** text edit box. After dismissing the dialog with the **OK** button the name of the new set will appear in the current technology menu.



Remark: the total number of device sets cannot exceed 30.

To delete one or more temporary device sets:

• To delete a temporary device set from the current technology menu, first select it from the menu, and then choose the **Select devices...** command from this menu. When the dialog with the list of components appears, click the **Remove set** button and dismiss the dialog with the **OK** button.

You can remove all temporary sets from the list by clicking the **Remove all sets** radio button and dismissing the dialog with the **OK** button.

Remark: it is not possible to delete permanent device sets. If the **Select devices...** command is chosen while one of the permanent sets is selected, the **Remove set** button will be inactive.

To define the default technology, default device set and/or to save the temporary device sets:

• Choose the **Save extractor settings** command from the **Options** menu.

This command modifies the EXCESS preference file. As far as technology is concerned, the consequences of executing the **Saue extractor settings** command are as follows:



- Current technology becomes the default technology
- Temporary device sets are stored in the preference file and will appear again in the technology menu when EXCESS is started and the default technology is read in.
- The selected device set becomes the default set (it can be either permanent or temporary).

3.1.4 Extraction of the electrical circuit

Extraction of the electrical circuit is performed in two phases.

Phase 1 (component extraction): Extraction of the components, finding their shapes, positions and dimensions.

Phase 2 (netlist extraction): Extraction of the circuit connectivity and device modeling.

It is possible to complete only the first phase and skip the second one. After the first phase it is possible to examine the layout visually. You can see the extracted IC components in the places where they have been found.

In the second phase, which can be executed after the first one, the circuit netlist is created and the output data are formated as a SPICE input file.

To run the component extraction:

Choose the **Circuit extraction** command from the **Run** menu. Extraction process will start. The *progress bar window* will appear and indicate the progress of the extraction.

After completion of this extraction phase the current technology menu will change. The list of device sets will be replaced by the list of extracted component classes.

To display the extracted components:

• Choose the name of the component class to be displayed from the current technology menu.

The layout drawing will be redrawn. All areas occupied by components of the selected type will be highlighted with the grey color.

To extract another set of components:

• Choose the **Next extraction** command from the **Run** menu.

This command will prepare EXCESS to start a new extraction process in the layout that is currently opened. After choosing this command you will be able to select a new device set from the current technology menu. Once the appropriate device set is selected, run the first phase of the extraction again by executing the **Circuit extraction** command from the **Run** menu.

To set network extracton options

• Choose the **Netlist...** command from the **Options** menu. The dialog box shown below will appear.



This dialog box allows you to set four parameters that affect the results of the extraction.

1. Parallel paths break coefficient. EXCESS can simplify the netlist if it finds two parallel current paths with large difference of resistance. In such a case the path with larger resistance can be removed from the network and a simpler equivalent circuit can be produced. The parallel paths break coefficient is the ratio of two resistances which, if exceeded, leads to simplification of the circuit. If you do not want to remove any resistance, set the coefficient to a very large value.

2. Minimum capacitance. In most cases extremely small capacitances do not affect the circuit functionality and performance. EXCESS can remove all capacitances below the minimum value and in this way simplify the network. If you do not want to remove any capacitor, set the minimum capacitance to a very small value.

3. MOS transistor division parameter. Large MOS devices cannot be modeled accurately in the same way as the small ones. The polysilicon gate behaves as a distributed RC network and the source and drain distributed resistances may also



n-SCM0S.exc

Mos trans.: Pchan

Mos trans,: Nchan



affect device characteristics. To account for these effects, EXCESS can divide big MOS devices into equivalent networks of smaller ones interconnected by resistors representing the gate, source and drain resistances. The MOS transistor division parameter determines the maximum allowed transistor aspect ratio. All transistors that exceed this value will be represented by equivalent networks of smaller transistors and resistances. The default MOS transistor division parameter value is zero. Zero means that the EXCESS transistor division option is switched off and no transistor will be divided. Of course, the same result can be achieved by setting this parameter to a very large value.

4. Diode model type. There are two ways of p-n junction diode modeling in EXCESS. The difference is in treating the junction sidewalls: either the junction is represented by a single diode, or the flat part of the junction and the sidewalls are modeled as two different diodes. In the second case the model parameters for the flat portion of the junction are different than the parameters for the sidewalls. This helps to improve the accuracy of modeling. However, both sets of model parameters (for the flat portion and for the sidewalls) must be defined in the technology file, otherwise the second option will have no effect.

The network options can be stored in the preference file by choosing the **Saue extractor settings** command from the **Options** menu.

To create output SPICE file:

Choose the **Output** command from the **File** menu. The standard dialog box for naming files to be saved will appear.



You can use this dialog to determine the name of output file that will be the input for the SPICE simulator.

Remark: The EXCESS output file is fully compatible with SPICE but it does not contain all the information necessary to run SPICE simulation (e.g. power supply, signal sources, list of nodes where voltages and currents should be observed and SPICE commands). You should add these data to the file using an external text editor.

3.2 Using menus in Extraction Mode

3.2.1 Apple menu

The Apple Menu contains one item related to EXCESS, followed by whatever desk accessories are included in the System file on the startup disk. It is the customary **About...** item that occurs in almost every Macintosh application.

About EXCESS...

This menu command displays the same startup dialog that can be seen upon invoking EXCESS. It tells who is the author of EXCESS and which version of EXCESS you use.

3.2.2 File menu

In the Extraction Mode, the **File** menu contains commands related to managing files with descriptions of technologies and IC layouts and circuits.

Open technology...

This command displays a dialog that enables you to open a technology file which describes the technology you want to use.

Close technology...

This command removes the current technology description from memory.

New technology

This command is used to enter the Technology Edit Mode and to start creation of new technology description.

Edit technology

This command is used to enter the Technology Edit Mode and allows to change the current technology description.

Open layout

This command displays a dialog that enables you to open a layout file you want to work with.

Close layout

This command enables you to remove the current layout from the memory and close the layout window. Before closing the layout you will be asked to confirm that you do not want to work with the current layout anymore.

Output

This command starts modeling of already extracted components and building of the circuit netlist. The netlist with the device models in SPICE format is written out to a file. This command is active if the first phase of extraction (invoked by the **Circuit extraction** command in the **Run** menu) has already been completed.

Quit

(keyboard equivalent '%Q')

This command quits EXCESS. EXCESS does not check whether any extraction has been performed or output file written. However, you will be asked to confirm that you do not want to work with the current layout anymore.

3.2.3 Edit menu

In the Extraction Mode the **Edit** menu contains only the standard commands but none of them is active. This menu is provided for compatibility with the MacOS standards.

3.2.4 Options menu

Save extractor settings

This command saves all current technology related settings: name of current technology file (it becomes default technology file), temporary device extraction sets, current extraction set (it becomes default extraction set) and network related settings.

Netlist...

This command displays a dialog which allows you to set some parameters that affect the results of the extraction.

3.2.5 View menu

The ${\tt View}$ menu contains commands that allow you to change the appearance of the mask artwork displayed in the layout window.

Turn Grid On/Off

This command toggles on and off visbility of the grid in the layout window. When the grid is switched on, a black dot is displayed at each grid point.

Grid Scale...

This command is used to change the distance between two adjacent grid dots.

Fit To Window

This command sets the drawing scale in the layout window so that the entire mask artwork fits exactly in the window.

Zoom In

This command enlarges the mask artwork drawing twice.

Zoom Out

This command reduces the mask artwork drawing twice.

3.2.6 Run menu

Circuit extraction

This command starts the first phase of the extraction, i.e. identification of the components and determination of their shapes and dimensions. Note that this command

does not create any output file. In order to obtain the SPICE netlist you have first to invoke the **Circuit extraction** command and then the **Output** command from the **File** menu.

New extraction

This command removes from the memory all results of an already performed extraction and prepares EXCESS for the next extraction (e.g. with another device extraction set).

3.2.7 Current technology menu

Before extraction this menu contains commands that allow to select a device set to be extracted and to define custom device sets. After extracton it contains a list of component classes that belong to the selected device set. If no technology is opened, this menu does not exist.

Select devices

This command displays a dialog that is used to create custom extraction device sets, to add them to the menu or to remove them from the menu.

Device set list

This is a list of extraction device sets. It contains names of all permanent sets and temporary sets. Selecting a set name from this list makes this set the current device set. The name of the current set is checked.

Component list

This is a list of names of component classes in the current device set. Choose a name in order to highlight all extracted components from this class in the layout window. All areas occupied by components that belong to the selected class will be filled with a light gray color or pattern.

3.2.7 Layout menu

This menu can be used to change the appearance of the mask artwork displayed in the layout window. It contains three commands and a list of names of all masks defined in the current technology. If no layout is opened, this menu does not exist.

Show all masks

This command makes all masks visible.

Hide all masks

This command makes all masks invisible.

Show/Hide labels

This command toggles on and off visibility of labels.

Mask list

This is a list of names of all masks that are used in the current technology. The mask names appear in the same color that is assigned to these masks in the technology file. Names of the masks that are currently visible in the layout windows are checked. Choose the name of a visible mask if you want to hide this mask. Choose the name of an invisible mask if you want to display it again. If the layout contains masks that are not defined in the technology file, these masks are displayed in black. You can hide or show them by selecting **all_others**, the last item in the mask list.

4 Technology Edit Mode Reference

The Technology Edit Mode is used to create and modify technology data files for use by EXCESS. Only one technology can be edited at a time.

EXCESS is not oriented towards any particular technological process used for manufacturing integrated circuits; however, it does have some built-in information about planar technology. This information is of a general nature and is applicable to all planar technologies. All information specific to technological process that is currently used is read by EXCESS from technology description files.

This chapter gives you information that is necessary for understanding the way EXCESS utilises technology description files. Most of the examples are based on a n-SCMOS technology (based on the public domain MOSIS scalable CMOS technology) with twelve technological masks:

- The nwell mask, which defines areas where n-doped well will be made and where pchannel transistors can be located.
- The active mask, which defines areas that will contain a thin layer of insulating silicon dioxide (gate oxide); the diffusion ¹ of dopants that will create sources and drains of MOS transistors may occur only in these areas.
- The polysilicon mask, which defines areas where the polysilicon layer will be deposited.
- The cut active mask, which defines openings in the silicon dioxide through which metal 1-diffusion contacts will be made.
- The cut_poly mask, which defines openings in the silicon dioxide through which metalpolysilicon contacts will be made.
- The pselect mask, which defines areas where p-channel transistors will be fabricated by use of p+ doping implantation. The same implantation is also used to enhance the doping concentration in p-doped substrate in the areas where contacts to the substrate will be made.
- The nselect mask, which defines areas where n-channel transistors will be fabricated by use n+ doping implantation. The same implantation is also used to enhance the doping concentration in n-doped wells in the areas where contacts to the wells will be made.
- The metal 1 mask, which defines areas where the first layer of metal will be deposited.
- The via mask, which defines openings in the silicon dioxide through which metal_1metal_2 contacts will be made.
- The metal_2 mask, which defines areas where the second layer of metal will be deposited.
- The glass mask which defines area where passivating silicon dioxide is usually deposited over integrated circuits to protect them from external chemical influences.
- The pad mask, which defines openings in the layer of passivating silicon dioxide. Through these openings, connections are made that provide a power supply to the integrated circuit, supply the input signals, and convey output signals to the outside.

You can find detailed descriptions of the CMOS technology in many VLSI textbooks.

In EXCESS, the technology description is composed of four separate but interrelated parts: masks, layers, devices, and device sets. These parts are briefly described below: Masks.

A mask is a set of geometrical data that allows to determine areas where a particular technological process can be activated. EXCESS uses the same mask sets that are used by manufacturers of integrated circuits.

Note: In EXCESS you can define technologies that contain no more than 32 masks.

¹ The term "diffusion" is used for historical reasons here. In all state of the art CMOS processes dopant atoms are introduced into silicon by means of ion implantation, not diffusion.

Layers.

In EXCESS layers are defined as areas that are created in silicon structure during technological processes and have a specific electrical property: can conduct electrical current in lateral (horizontal) direction. In every typical IC structure there are several types of such layers:

- substrate layer n or p-doped silicon where wells of the opposite dopant type and transistors of the opposite channel type can be located,
- well layer n or p-doped area of silicon that can be treated as substrate for transistors of the channel type opposite to the well type,
- polysilicon layer polysilicon paths,
- metal layer metal paths,
- diffusion layer the definition of this layer is more complicated than definitions of the layers that have been listed above. The intuitive meaning of this layer is that it is either a n-doped or a p-doped path in silicon that has been created by implanting dopant atoms into an area selected by active mask. If an active area is crossed by a polysilicon path, a transistor channel instead of a doped path will be created under the polysilicon. In EXCESS the "diffusion layer" name is applied to the whole area where both doped paths and transistor channels can be potentially created (the polysilicon mask determines how the diffusion layer will be divided into transistor channels and doped paths).

In a typical IC technology there is only one substrate layer. The number of other layers depends on the details of the technology. For example in the n-SCMOS technology there are: one p-type substrate layer, one n-well layer, two diffusion layers (p and n), one polysilicon layer and two metal layers.

Although layers may have the same names as masks, do not confuse layers with masks. EXCESS layers correspond to physical layers created in technological processes that may involve several masks and processing steps. As a result, the geometry of areas of a particular layer is not necessarily identical with geometry of areas on the mask with the same name.

Devices.

There are two basic types of circuit components, also called devices, in the EXCESS technology definition:

- Single layer devices that are created within a single layer. There are two classes of devices that can be created within the metal and polysilicon paths: resistors (resistance of a path) and capacitors (lateral capacitance between two adjacent paths of the same layer). Substrate, well and diffusion layers can be characterised only by one device class: parasitic resistance.
- Composite devices that are created by a specific interaction between a pair of paths of two different layers. The nature of this interaction often additionally depends on a combination of some masks in the device area. For example an overlap of the polysilicon and metal1 paths can create either a contact or a capacitor, depending on the poly_cut mask. If there is an opening in the poly_cut mask, a contact will exist, otherwise the paths will be separated by a dielectric layer and the overlap will become a capacitor. There are four types of composite devices: contacts, capacitors, transistors and diodes.

Note: the definition of devices should be complete, i.e. all devices that may exist in a given technology should be defined in the technology file.

Device sets.

Not all classes of devices that are defined for a given technology must be included in the extracted circuits. A subset of all classes of devices that can be extracted in a given technology is called a device set. Depending on the nature of a device, devices that are not included in a particular set are either deleted from the extracted network (capacitors, diodes) or replaced by electrical connections (resistors).

It is possible to define up to 30 different sets of devices. It is usually convenient to define at least three sets:

- full all device classes are included,
- nominal only MOS transistors are included, parasitic devices are not included,
- optimal MOS transistors and the most important parasitic devices is included.

Each part of the technology description is edited in a different type of window. The remainder of this chapter tells you how to define a new technology using appropriate edition windows.

4.1 Working with EXCESS in Technology Edit Mode

EXCESS starts up in the Technology Edit Mode if it is invoked to open and edit an existing technology file. To create a new file, start EXCESS alone and enter the Technology Edit Mode by choosing the **New Technology** command from the **File** menu. After entering the Technology Edit Mode a new menu bar will appear:

🐞 File Edit Definitions

4.1.1 Manipulating technologies in Technology Edit Mode

To open and edit an EXCESS technology data file from the Finder or create new one:

Start up EXCESS and enter the Technology Edit Mode as described in Section 3.1.1 or in the beginning of this chapter.

To save the currently edited technology:

• Choose the **Saue** command from the **File** menu.

The **Save** command writes to the disk the currently edited technology. If the currently edited technology was created using the **New Technology** command, a dialog box will appear, asking where to save it.

Possible problems:

If the currently edited technology has not been changed since it was saved, the save command is inactive.

To change the name of a technology:

Choose the Save as... command from the File menu.
 The standard dialog box will appear. Enter the new name and press the Save button. A new technology file will be created. You can remove the old technology file from the Finder by moving it to the Trash.

File		
Save	兼ら	
Save As		
Extraction Mode		
Quit	жQ	

Note: The name of the technology description file is treated as technology name. It is used to inform which technology you currently use in menus, windows, dialog boxes etc. The only way to change the technology name is to change the name of the technology file. You can do that as described above or you can do that from the Finder.

To quit Technology Edit Mode:

• To quit EXCESS directly from Technology Edit Mode select the **Quit** command from the **File** menu.

To quit Technology Edit Mode and go to Extraction Mode without quitting EXCESS select the **Extraction Mode** command from the **File** menu.



Note: If currently edited technology was created using the **New Technology** command or if you have changed something in an old technology, you will be asked to save the technology file.

4.1.2 Defining masks

•

To start mask definition procedure:

• Select the Mask Definition... command from the Definitions menu.



The dialog that contains list of masks in the current technology will be displayed. You can add or remove masks and change their attributes using this dialog.



To add a new mask:

- Click the **Add** button. The mask definition dialog will be displayed (See Mask definition dialog later in this chapter).
- Note: The position of the new mask on the mask list can be determined by selecting one of existing masks before pressing the **Add** button. New mask will be added after the selected mask. If no mask is selected, the new one will be added as the first mask on the list.

To remove a mask:

• Select the mask that you want to remove from the list and click the **Remove** button.

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nvell active polysilicon cut_active cut_poly pselect nselect metal_1 via metal_2	Add Remove Open	
glass pad	Cancel	

To edit mask definition:

Select the mask that you want to edit and click the **Open** button. The mask definition dialog will be displayed.

Mask definition dialog

After pressing ${\tt Add}$ or ${\tt Open}$ button in the mask list dialog the mask definition dialog will be displayed:



You can use this dialog to determine some attributes of the mask:

- mask name;
- CIF name of the mask. This name is assigned to the mask in CIF layout description format.
- Mask display color. This color will be used to display the mask in the layout window. You can change this color by clicking the color rectangle. The standard Macintosh color picker dialog will be displayed.
- Note: Definition of statistical characteristics of random mask disturbances is reserved for EXCESS Statistical a version of EXCESS which can simulate random disturbances of litography processes such as mask misalignment, over/underetching and spot defects.
- IMPORTANT: Definitions of layers, devices and device sets are based on the definition of masks. Significant changes in the definition of masks (number of masks, mask names, sequence of masks on the list) will invalidate the definitions of layers, devices and device sets. These definitions will be completely deleted.

4.1.3 Defining layers

To start layer definition procedure:

 Choose the Layer Definition... command from the Definitions menu.

Definitions		
Mask Defi	nition	
Layer Definition 🕟		
Composite Devices		
Device Sets		
Settings		

The dialog that contains a list of layers in the current technology will be displayed.

п-SCM0S.екс		
Meta12 Meta11 Polysilicon Pdiffusion Ndiffusion Nwe11 substrate	Add Remove Open	
	Cancel T	

You can manipulate layers using this dialog in the same way as manipulating masks, i.e. you can add and remove layers and edit their attributes in the layer definition dialog.

IMPORTANT: The sequence of layers on the list must correspond to the "physical" sequence of layers in the semiconductor structure from the top of the struture to the substrate. In other words, the upper metal layer should be the first one and the substrate layer should always be the last one.

Layer definition dialog:

After clicking either ${\tt Add}$ or ${\tt Open}$ button in the layer list dialog the layer definition dialog will be displayed:



You can use this dialog to:

- determine how the masks are used in the manufacturing process to create this layer,
- define basic physical and electrical attributes of the layer,
- define single layer devices.
- Basic attributes of the layer are:
 - Layer name.
 - Physical parameters. These parameters are used by EXCESS to calculate some electrical values (fringe capacitances, edge diode areas etc). There are three physical parameters:
 - thickness (in micrometers): for metal and polysilicon layers the actual layer thickness, for wells and diffusions the junction depth. Layer thickness should not be set to zero.
 - Minimal width (in micrometers): determined in the design rules of your technology.
 - Typical distance from the substrate (in micrometers) you can calculate it from thickness of dioxide layers in your technology. This parameter should be greater than zero for metal and polysilicon layers. It should be set to zero for the other layers (diffusion, well, substrate).
 - Layer conductivity. This parameter is used by EXCESS to determine the transistor types (n-channel or p-channel) or the polarity of diodes. There are three different types of conductivity that you can choose for the layer:
 - conductor for metal and polysilicon layers,
 - p-type semiconductor for substrate, diffusion and well layers,
 - n-type semiconductor for substrate, diffusion and well layers.
- Single layer devices:
 - Resistor. You should define the name of this device and its basic electrical parameter the sheet resistance. Sheet resistance equal to zero means that the layer should be treated by EXCESS as ideal conductor (equipotential wire). A nonzero value tells EXCESS that the layer introduces parasitic resistances.

- Note: It is recommended that all layers should have nonzero sheet resistances. If you decide later that you want to neglect the parasitic resistances introduced by this layer, you will be able to remove them from the set of devices to be extracted. This will automatically change these parasitic resistances into equipotential wires (See "Setting the subset of components to be extracted" Section).
- Capacitor. There are three parameters that you should determine:
 - Capacitor name,
 - Relative dielectric permittivity of the dielectric layer that surrounds the conducting layer (typically silicon dioxide with permittivity equal to 3.82),
 - Maximum radius (in micrometers) this tells EXCESS how far it should look for a path adjacent to the current one in order to extract a lateral capacitor. If the maximum radius is too large, the extracted circuit will include large number of extremely small lateral capacitances which will usually have no noticeable effect on the operation of the circuit. Set the maximum radius to zero if you do not want to extract lateral capacitors on the layer. Lateral capacitors should be defined only for metal and polysilicon layers. It makes no sense to define lateral capacitances for well or diffusion layers because there is no lateral capacitance between two adjacent wells or diffusions. Therefore, for these layers the maximum radius should be set to zero. Well and diffusion layers create p-n juctions (e.g. n-diffusion to p-substrate or p-diffusion to n-well). There are parasitic capacitances associated with these junctions. These capacitances are accounted for in the junction diode models (See "Defining composite devices" chapter).
- Note: It is recommended that the maximum radius is not set to zero for the polysilicon and metal layers. If you decide later that you want to neglect the lateral capacitances introduced by a layer, you will be able to remove these capacitances from the set of devices to be extracted. (See "Setting the subset of components to be extracted" Section).
- Definition of the relationship between the masks and the layer:

Some layers are created in one litography process involving a single mask. Well and metal layers usually belong to this class of layers. Other layers are created in a number of processing steps. The shapes on such layers are defined by more than one mask. To define the relationship between the masks and the layer means to define a Boolean expression which tells EXCESS how the masks are used in order to create shapes on the layer. The contours on each mask divide the whole layout area into areas where a technological process affects the semiconductor structure (e.g. a dopant is introduced) (Boolean value of these mask areas: true) and areas which are not affected (Boolean value of these mask areas: false). If a single mask is used, the Boolean expression is simple and obvious. If more than one process and mask is involved, a more complex expression is needed. For example n-diffusion layer is created in areas common to "active" and "nselect" masks. Therefore, the corresponding Boolean expression is: "active" and "nselect".

In the n-SCMOS technology there is no need to use more complicated expressions, but in general you can create any Boolean expression involving "and" and "or" operators and mask names as operands.

To define mask expression for a layer:

Click the **Edit** button in "Mask expression" box. The mask expression dialog will appear. This dialog is used to define implicants of the mask expression, one at a time. The final mask expression has always the general form: "implicant_1 or implicant_2 or implicant_3 or ...", where implicants are expressions of the form "mask_1 and mask_2 and mask_3 and ...".



To the left there is a list of masks, to the right the current mask implicant – a part of the mask expression with "and" operators only. To define an implicant in an open window, select appropriate mask names, one at a time, in the mask list and use the **Add mask affirmation>>**, **Add mask negation>>** and **<<Remove mask** buttons as necessary. To create a new implicant click the **Add** button. A new window associated with the new implicant will be displayed. You can work with the set of implicants using the **Show previous**, **Show next**, **Add** and **Remove** buttons. Click the **OK** button when all implicants are correctly defined.

- Note: the substrate layer is created by EXCESS automatically and has a special meaning. It cannot be removed and you should not attempt to define any expression for it. The only parameter you should specify is the type of conductivity (either n-type or p-type semiconductor).
- IMPORTANT: Definitions of devices and device sets are based on the definitions of layes. Singificant changes of the definitions of layes such as change of number of layers, their sequence, their mask expressions, definitions of single layer devices etc. will invalidate the definitions of devices and device sets. These definitions will be completely removed.

4.1.4 Defining composite devices

Definition of composite devices is the most complex and time consuming task. Composite devices are created at intersections of paths that belong to two different layers. The device type is usually determined by the types of layers that intersect each other and either presence or absence of some masks in the intersection area.

To start composite device definition procedure:

• Choose the **Composite Devices...** command from the **Definitions** menu.



The dialog that contains a list of all pairs of layers in the current technology will be displayed:

n-SCMOS.exc			
Layers in interaction	Devices		
Metal2-Metal1	Cipen		
Dpen	Cancel OK		

Composite devices are created by interactions between pairs of paths from different layers. Every pair of layers can produce such devices. EXCESS generates automatically all possible pairs of layers and places these pairs onto the list "Layers in interaction". You cannot add new pairs or remove existing ones.

For every pair of layers you should define the set of devices that can be created. Since specific layer interaction is often determined by one or more additional masks (usually contact masks), for every pair of layers EXCESS creates a special structure for defining composite devices. It is a binary tree structure. The root node of the tree is assigned to a pair of layers, and the intermediate nodes are assigned to masks. The leaf nodes are assigned to devices, and all other nodes have the "not a device" attribute. An example of such a tree is shown schematically below:



This schematic shows that there are four composite devices defined for the current pair of layers with additional usage of three masks (1, 2 and 3):

- device A is created with usage of mask 1 and mask 2 (mask Boolean expression: "mask 1 and mask 2"),
- device B is created with usage of mask 1 and mask 2 (mask Boolean expression: "mask 1 and not mask 2"),
- device C is created with usage of mask 1 and mask 2 (mask Boolean expression: "not mask 1 and not mask 2"),
- device D is created with usage of mask 1, mask 2 and mask 3 (mask Boolean expression: "not mask 1 and mask 2 and mask 3"),

In practice the binary trees are less complicated than in the example shown above. The figure below shows the most complex tree in the n-SCMOS technology. It defines composite devices between the metal1 and polysilicon layers.



Working with composite devices binary tree

To start working with composite devices binary tree, select one of the layer pairs listed in the left part of the dialog. The list in the right part of the dialog displays all devices that have been already defined for the selected pair of layers.



You can start visiting an existing tree from its root node by clicking the **Open** button below the "Layers in interaction" list or you can go to a leaf node of the tree by selecting a device and clicking the **Open** button below the "Devices" list. When you select the root node, you will see the device tree edition dialog:



You are at the root node which has the attribute "not a device". If no device is defined at a node ("not a device" in the pop-up menu in the "Device specification" box), the current node is not the leaf node and the definition of a device is not finished yet. In the part of the dialog entitled "Masks to be used" there is a list of all masks. By selecting a mask from this list you choose the next node of the tree. To choose an existing node, click the **Open** button (in either "Affirmation" or "Negation" box).



You are now at the leaf node which defines parasitic resistance of the metal1-polysilicon contact. Since this is the leaf node, the "Mask to be used" list is inactive. The "Masks prev. used" list shows the sequence of masks that has been defined previously for the current device (from the root node through all tree levels), and in the **Device** pop-up menu you can see the device type assigned to this node.

By choosing the **Not a device** item from the **Device** pop-up menu you can tell EXCESS that this is not the leaf node, and the definition of a device is not completed yet. If the "not a device" attribute is set, the "Mask to be used" list is active and the next node can be defined, as shown below.

Metal1-Polysilicon		
Composite layer modification		
Masks prev. used Masks to be used out_poly Image: Create (Bpen) Image: Create (Bpen) Image: Create (Bpen)		
Device specification Cancel Device: Not a device Model OK		

Defining devices:

To define a composite device, choose the appropriate device type from the **Device** pop-up menu and then define its electrical parameters by clicking the **Model** button. The model definition dialog will appear. The appearance and function of this dialog depends on the type of device to be defined.

There are five types of composite devices:

• Contact:

This is a connection between two layers with zero resistance. There is no electrical model of this component.

• Resistor:

This is a resistive connection between two layers. In the model of this device you can define its name and the contact resistance:



Note: It is recommended to define all contacts as resistive devices. If such a device is not selected in an extraction device set, it will be treated as a nonresistive contact.

• Capacitor:

It represents capacitance between two layers. In the model of this device you can define its name and capacitance per unit area:

Capacitor name:	CM1Poly
Capacitance [F/sq.cm]:	4.9e-09
	Cancel OK

• Diode:

The SPICE diode model is implemented. In the model definition dialog there are two lists. The left one is a list of all SPICE diode model parameters. The right one is a list of parameters selected for output. In the EXCESS output file only the parameters that appear on the right list will be included in the diode model. To add a parameter to the output list, select it on the left list and click the **Add** button. The name of the parameter will appear on the output list and the definition of this parameter will be

displayed in the middle of the dialog. A value should be assigned to this parameter in the text edit box. To remove a parameter from the output list, selecting it on the output list and click the **Remove** button.



It is possible to define a different model for the edge (sidewall) part of the diode. If such a model is defined, every extracted p-n junction will be represented by two diodes: one representing the flat portion of the junction, and another representing the sidewalls. To define the model for the edge diode, click the **Edge part model** button to obtain the model definition dialog for the edge diode.

• MOS transistor:

The MOS transistor model is defined in the same way as the diode model. The predefined set of parameters allows you to define any of the three standard SPICE MOS transistor models.



IMPORTANT: If you change the number or names of composite devices, the definitions of extraction device sets will no longer be valid. These definitions will be completely removed.

4.1.5 Defining device sets

To start definition of extraction device sets:

• Choose the **Device Sets...** command from the **Definitions** menu.



The dialog that contains a list of permanent device sets in the current technology will be displayed.



You can add a new device set by clicking the **Add** button, remove an already defined set by clicking the **Remove** button, and edit an already defined set by clicking the **Open** button. If you click the **Add** or **Open** button, the device set definition dialog will appear.

Remark: In the list of existing extraction device sets you will see permanent sets as well as temporary sets defined as described in the Setting the subset of components to be extracted Section. The temporary sets are stored in the preference file, not the technology file. However, if you save the technology file while some temporary sets are defined, they will become permanent.

Device set definition dialog



The names of devices currently included in the set are highligted. To add a device to the set, select it on the list by clicking its name while the OPTION and SHIFT keys are depressed. To delete a device from the set, deselect it in the same way. Once the set is correctly defined, dismiss the dialog with the $\mathbf{0}\mathbf{K}$ button.

4.1.6 Defining the standard network extraction options

Choose the **Settings...** command from the **Definitions** menu.

The dialog will be displayed. It can be used to set the standard values of four parameters that affect the results of the extraction.



1. Parallel paths break coefficient. EXCESS can simplify the netlist if it finds two parallel current paths with large difference of resistance. In such a case the path with larger resistance can be removed from the network and a simpler equivalent circuit can be produced. The parallel paths break coefficient is the ratio of two resistances which, if exceeded, leads to simplification of the circuit. If you do not want to remove any resistance, set the coefficient to a very large value.

2. Minimum capacitance. In most cases extremely small capacitances do not affect the circuit functionality and performance. EXCESS can remove all capacitances below the minimum value and in this way simplify the network. If you do not want to remove any capacitor, set the minimum capacitance to a very small value.

3. MOS transistor division parameter. Large MOS devices cannot be modeled accurately in the same way as the small ones. The polysilicon gate behaves as a distributed RC network and the source and drain distributed resistances may also affect device characteristics. To account for these effects, EXCESS can divide big MOS devices into equivalent networks of smaller ones interconnected by resistors representing the gate, source and drain resistances. The MOS transistor division parameter determines the maximum allowed transistor aspect ratio. All transistors that exceed this value will be represented by equivalent networks of smaller transistors and resistances. The default MOS transistor division parameter value is zero. Zero means that the EXCESS transistor division option is switched off and no transistor will be divided. Of course, the same result can be achieved by setting this parameter to a very large value.

4. Diode model type. There are two ways of p-n junction diode modeling in EXCESS. The difference is in treating the junction sidewalls: either the junction is represented by a single diode, or the flat part of the junction and the sidewalls are modeled as two different diodes. In the second case the model parameters for the flat portion of the junction are different than the parameters for the sidewalls. This helps to improve the accuracy of modeling. However, both sets of model parameters (for the flat portion and for the sidewalls) must be defined in the technology file, otherwise the second option will have no effect.

Appendix A CIF file format

EXCESS accepts full CIF 2.0 format as described in literature.

EXCESS requires top cell call (line: C top_cell_number; should be always placed in the file). Labels description format is shown below:

94 text_name x_coordinate y_ coordniate [layer_name];

Appendix B Known bugs and problems

Excess occasionally crashes when opened together with some other, probably buggy, applications. This does not seem to be a problem within EXCESS. To avoid such crashes, avoid using ECXESS together with applications of questionable quality (shareware, beta versions, etc.).

EXCESS may also crash when opening extremely large layouts. Enlarging the amount of memory sometimes, but not always, helps. We are working on fix of this problem.